Design Example Report

Title	*70 W Output Automotive Power Supply for 400 V Systems Using InnoSwitch™3-AQ INN3949CQ*
Specification	190 V_{DC} – 450 V_{DC} Input; 14 V / 5 A Output
Application	µDCDC / 12 V Battery Replacement
Author	Automotive Systems Engineering Department
Document Number	DER-1035Q
Date	February 26, 2024
Revision	1.0

Summary and Features

- Ultra-compact design for 400 V_{DC} BEV automotive applications
- Low component count (only 66 components)[1] design with a single 1700 V power switch
- Full load operation from 190 V_{DC} to 450 V_{DC} input[2]
- Reinforced 450 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥94% full load efficiency across the input voltage range
- 1% output voltage load and line regulation
- Secondary-side regulated output
- Ambient operating temperature from -40 °C to 85 °C
- Complete fault protection, including output current limit and short-circuit protection
- Uses automotive-qualified AEC-Q surface mounted (SMD) components[3]
- Low profile, 30 mm height

[1] Power conversion stage only, excluding input and output ports. See Figure 5
[2] Derated power below 190 V_{DC} input. See Figure 86
[3] AEC-Q200 transformer qualification and AEC-Q qualified SR MOSFET selection belong to final design.

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Table of Contents

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1 Introduction

This engineering report describes a 70 W single-output automotive power supply intended for 400 V battery system electric vehicles. The design supports a wide input range of 190 V_{DC} to 450 V_{DC}. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (output) sides by observing the creepage and clearance requirements according to IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic diagram, printed circuit board (PCB) layout, bill of materials (BOM), magnetics specifications, and performance data.

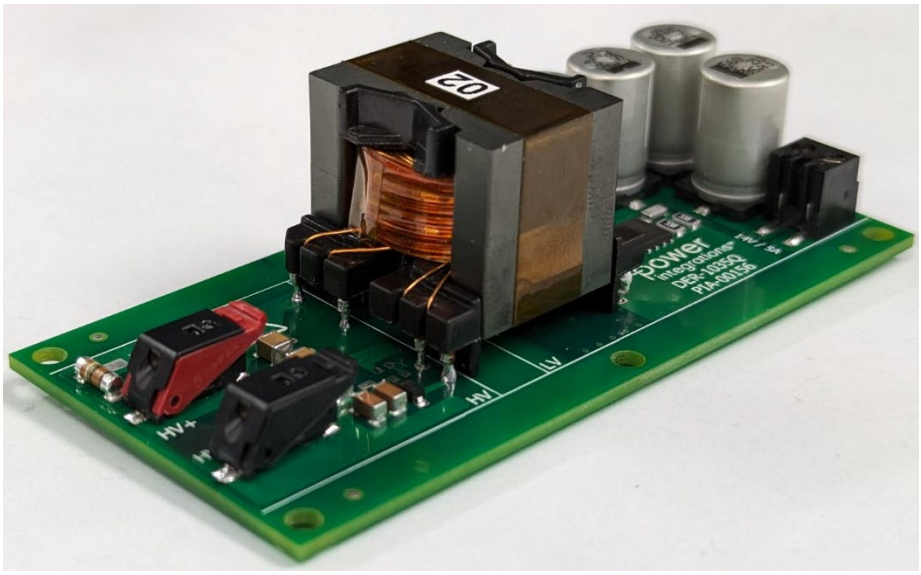


Figure 1 – Populated Circuit Board, Entire Assembly.

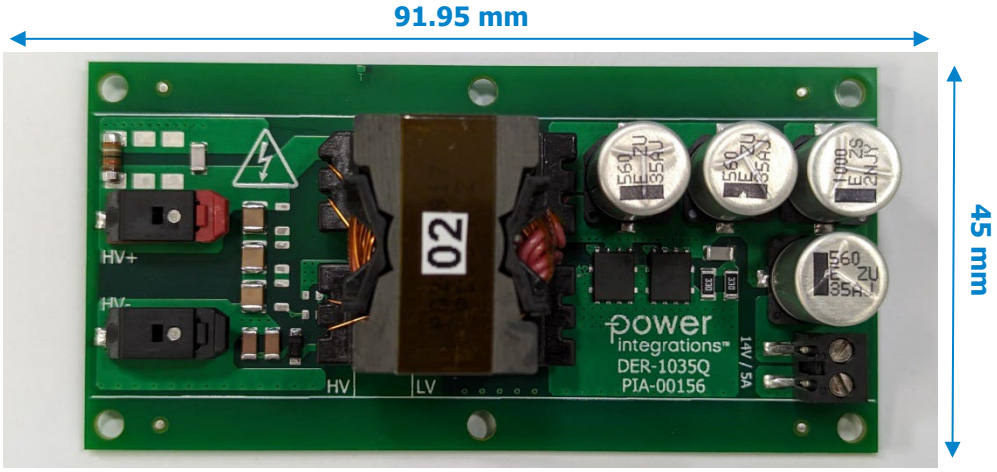


Figure 2 – Populated Circuit Board, Top.

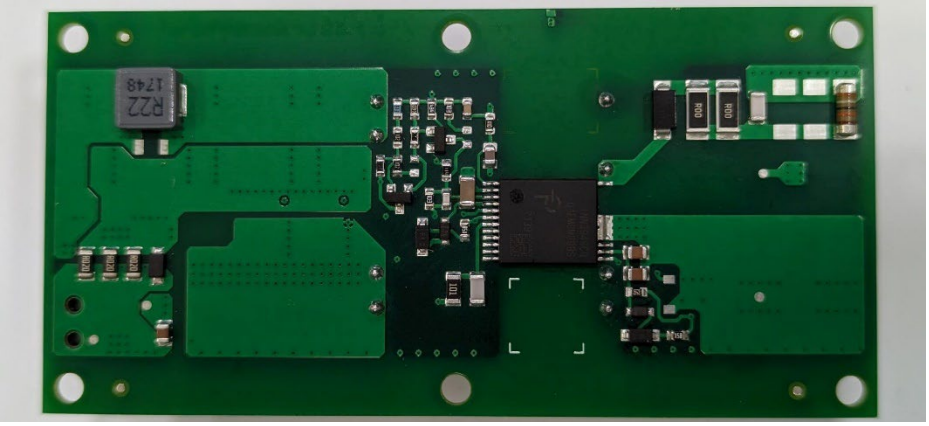


Figure 3 – Populated Circuit Board, Bottom.

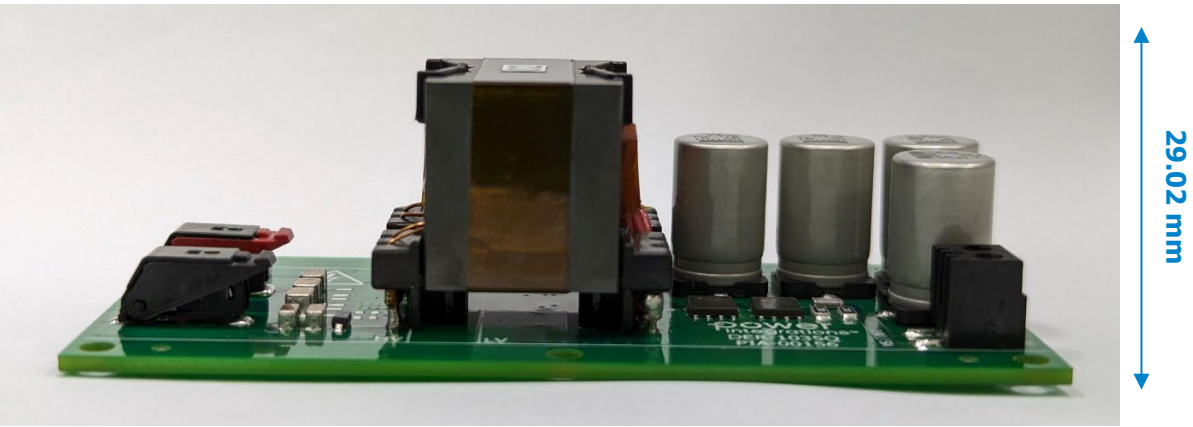


Figure 4 – Populated Circuit Board, Side.

The design can deliver continuous 70 W output power at 85 °C ambient temperature from 190 V_{DC} to 450 V_{DC} input voltage range. The 14 V output configuration allows the design to replace a vehicle's auxiliary battery, helping reduce weight and lessen maintenance.

The InnoSwitch3-AQ IC maintains necessary regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary side via FluxLink™. Secondary-side controls synchronous rectification for improving the overall efficiency compared to diode rectification, thus saving cost and space by eliminating the need for a heat sink.

2 Design Specification

The following tables below represent the performance of the design.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	190[4]	300	450	V_{DC}
Operating Switching Frequency	**f_{SW}**	25		52	kHz
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	**V_{OUT}**	13.8	14	14.2	V_{DC}
Ripple Voltage Measured on Board	**V_{RIPPLE}**			150	mV
Output Current Parameters					
Output Current	**I_{OUT}**		5000		mA
Output Power Parameters					
Continuous Output Power at 150 V_{DC} – 500 V_{DC} Input	**P_{OUT}**		70[5]		W
Output Overshoot and Undershoot During Dynamic Load Condition	**ΔV_{OUT}**	-200		200	mV

Table 1 – Electrical Specifications.

[4] Lower input voltage is possible but with output power derating.
[5] For maximum output power capability at V_{IN} less than 190 V, see Section 13.

2.2 Isolation Coordination

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	$\mathbf{BV_{DSS}}$			1700	V
System Voltage	$\mathbf{V_{SYSTEM}}$			720	V
Working Voltage	$\mathbf{V_{WORKING}}$			450	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175			
Rated Impulse Voltage	$\mathbf{V_{IMPULSE}}$			2.5	kV
Altitude Correction Factor for h_a	**Cha**	1.59			
Basic Clearance Distance Requirement	$\mathbf{CLR_{BASIC}}$	2.4			mm
Reinforced Clearance Distance Requirement	$\mathbf{CLR_{REINFORCED}}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$\mathbf{CPG_{BASIC(PCB)}}$	3.6			mm
Reinforced Creepage Distance Requirement for PCB	$\mathbf{CPG_{REINFORCED(PCB)}}$	7.2			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	$\mathbf{V_{ISO}}$	5000			V_{PK}
Partial Discharge Test Voltage	$\mathbf{V_{PD\_TEST}}$	1080			V_{PK}

Table 2 – Isolation Coordination[6].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	°C
Altitude of Operation	ha			5500	m

Table 3 – Environmental Specifications.

[6] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

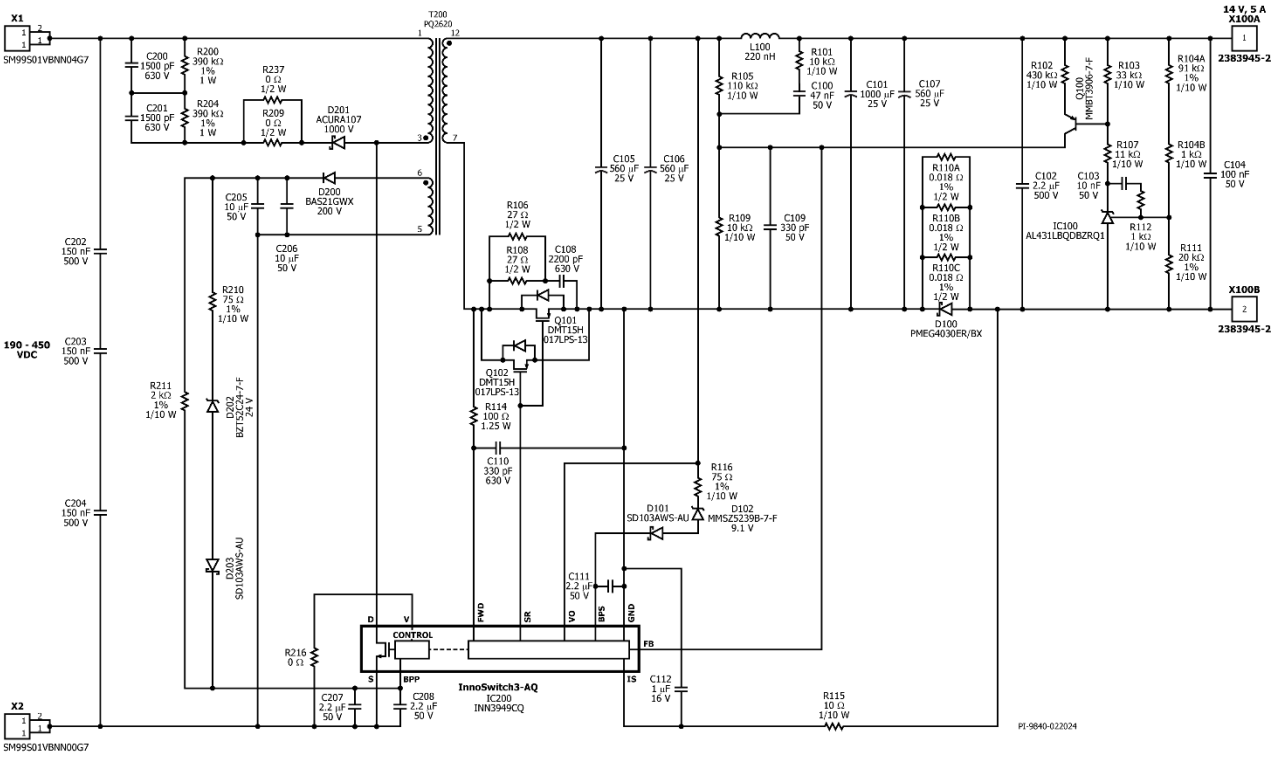


Figure 5 – DER-1035Q Power Conversion Stage.

4 Circuit Description

4.1 High-Voltage Side Circuit

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from the high-voltage input. The flyback transformer T200 primary winding is connected across the high-voltage DC input and the drain terminal of the 1700 V SiC power MOSFET switch internal to the INN3949CQ IC (IC200).

An R2CD-type snubber circuit is placed across the primary side winding to limit the drain-source voltage peaks seen by the internal SiC MOSFET switch during turn-off. A super-fast (or better) surface mount, AEC-Q qualified diode should be used. Diode D201 meets creepage and clearance requirements and ensures that the reverse voltage across the diode would not exceed 70-75% rating. Capacitors C200 and C201 catch the energy from the leakage inductance of transformer T200. The capacitor values are selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation throughout the switching period. Resistors R200 to R204 dissipate the energy stored by the snubber capacitors. The resistor values are selected such that their average voltage will not exceed 80% of their voltage rating and dissipate less than 50% of their rated power.

IC200 is self-starting, using an internal high-voltage current source to charge the BPP capacitor (C207 and C208).

The transformer T200 auxiliary winding provides power to the primary side of IC200 during normal operation. This minimizes the power derived from the internal high-voltage current source, improving overall efficiency, and reducing heating of IC200. The auxiliary winding output is rectified and filtered by diode D200 and capacitors C205 and C206. Current is fed to the BPP pin through resistor R211.

4.2 InnoSwitch3 Input Undervoltage

The V pin of the IC200 INN3949CQ IC is used to provide line undervoltage on/off.

The IC200 INN3949CQ IC is enabled when the current injected into the V pin is above the UV pin brown-in threshold (I_{UV+} = 27 µA), it is turned off otherwise. The V pin is connected to HV RTN by default using jumper resistor R216 to disable UV, but additional provisions for UV setting are included. Resistors R212 to R214 must be calculated such that the current injected into the V pin is above the brown-in threshold after D204 clamps the voltage between R214 and R215.

4.3 Low-Voltage Side Circuit

The secondary-side of the INN3949CQ IC (IC200) provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q101 and Q102 rectify the voltage across the secondary winding of the transformer T200, which is then filtered by output capacitors C105 to C106. An RC-type snubber formed

by resistors R106 and R108 and capacitor C108 dampens the high-frequency ringing in the SR FET drain-source nodes.

The secondary-side controller inside IC200 controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed from the FWD pin via resistor R114. Capacitor C110 and resistor R114 form a low pass filter that reduces the voltage spike seen by the FWD pin during SR turn-off and ensures that the maximum rating of 150 V will not be exceeded.

In continuous conduction mode, the SR gate signal is turned off before the secondary-side controller requests a new switching cycle to the primary. In discontinuous conduction mode, the SR FET is turned off when the voltage across it falls below $V_{SR(TH)}$[7]. Secondary-side control of the primary-side power MOSFET removes the possibility of cross-conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary-side of IC200 is powered by either the secondary winding forward voltage (thru R114 and the FWD pin) or the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C111 via an internal regulator.

Diodes D101, D102, and resistor R116 serve as a secondary-side output overvoltage protection (secondary OVP). During output overvoltage events, current will be injected to the BPS pin of IC200 through these components and triggers the IC to operate in auto-restart (AR) mode.

The INN3949CQ IC has an FB pin internal reference of 1.265 V. Resistors R105 and R109 form the basic voltage divider feedback network for InnoSwitch3-AQ designs. For this design, the output voltage value set by R105 and R109 is 10-15% higher than the rated output voltage as a requirement for implementing the *Precise Voltage Regulation* circuit. Capacitor C109 provides decoupling from high-frequency noise affecting power supply operation. Capacitor C100 and resistor R101 form a feedforward network to speed up the feedback response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across parallel resistors R110A to R110C. The resulting current measurement is filtered using R115 and C112 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of around 35 mV is used to reduce losses. Once the threshold is met, IC200 will control the number of pulses to maintain a fixed output current. The IC enters auto-restart (AR) operation when the output voltage falls below 90% of regulation and recovers when the load current is reduced below the CC limit. Diode D100 limits the voltage drop across R110A to R110C to protect the IS pin during overload or short-circuit conditions.

4.4 Precision Voltage Regulation (PVR) Circuit [8]

The PVR circuit improves output voltage regulation by using an external error amplifier with a high-precision reference voltage (ATL431) to control the FB pin. The PVR injects a DC bias current to the FB pin of IC200 to reduce the DC error at the output. The ATL431

[7] Refer to InnoSwitch3-AQ datasheet for $V_{sr(TH)}$

[8] Circuit implementation is only necessary if output voltage regulation needs to be within 1%.

error amplifier network is placed after the output filter inductor L100 and current sense resistors R110A to R110C to compensate for voltage drops.

The ATL431LIBQDBZRQ1 is selected for its high precision and stability across temperatures. The output voltage is sensed through voltage dividers R104A, R104B and R111. The resistor values are chosen such that at the rated output voltage, the voltage across the REF pin of IC100 equals the reference voltage of 2.5 V. IC100 sinks cathode current proportional to the difference between the scaled output voltage and its internal reference. The amount of cathode current affects the amount of current injected into the FB node. Capacitor C103 lowers the bandwidth of the PVR circuit so that it only corrects for DC error.

Resistors R103 and R107 provide the base current path for Q100 and bias current to IC100. Together with R102, the values of these resistors are chosen such that IC100 and Q102 are kept away from saturation and provide an adequate allowance for the base and cathode currents to swing during load transients. While operating in the forward active region, it can be interpreted that Q100 acts as a variable impedance in parallel to the upper feedback resistor R105.

5 PCB Layout

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

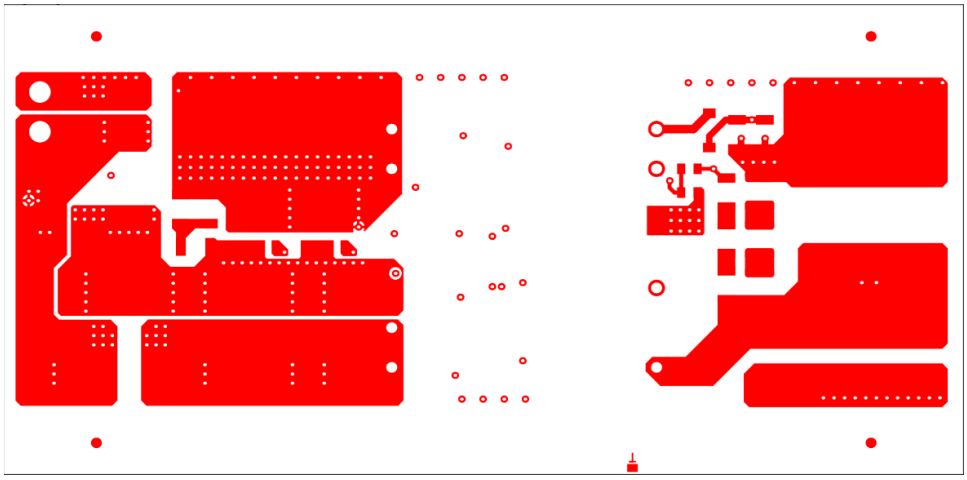


Figure 6 – DER-1035Q Top Layer PCB Layout.

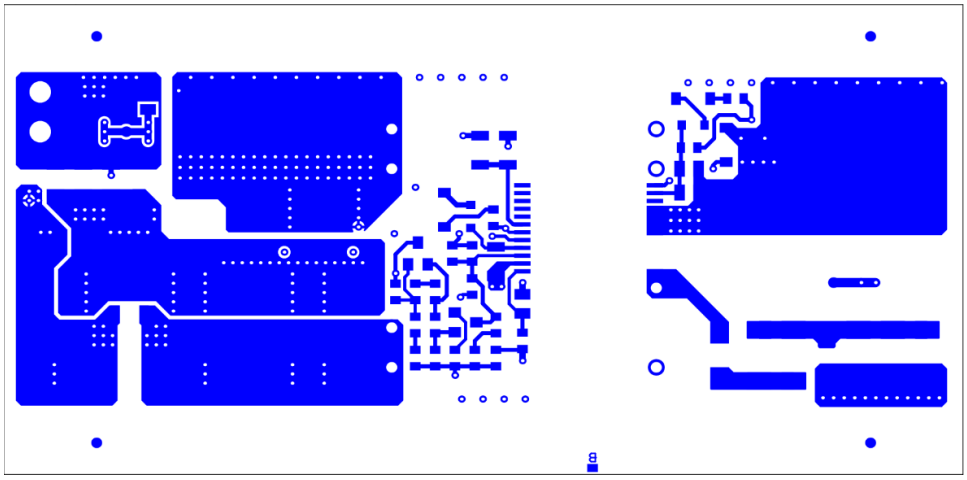


Figure 7 – DER-1035Q Bottom Layer PCB Layout.

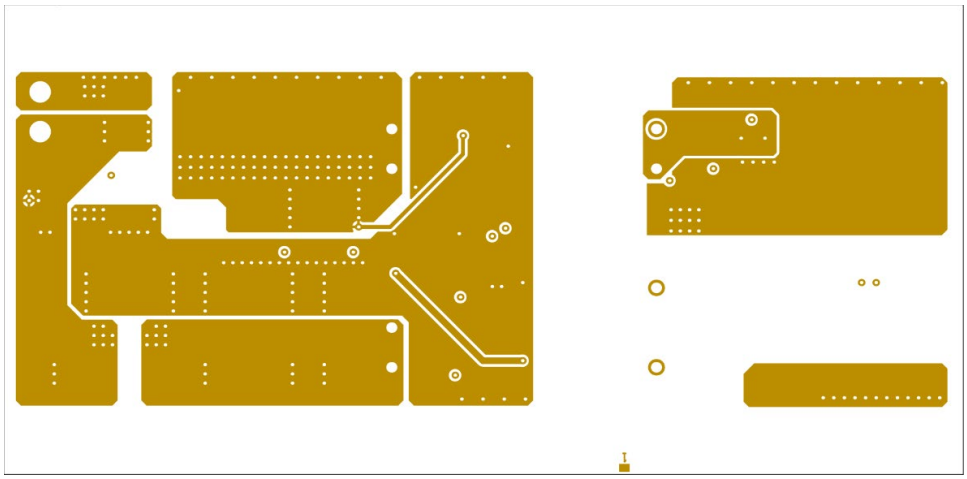


Figure 8 – DER-1035Q Mid-Layer 1 PCB Layout.

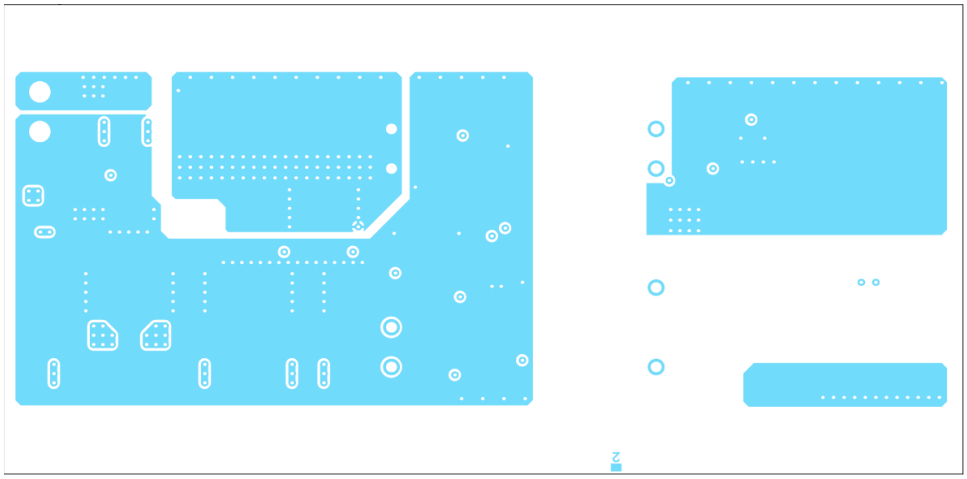


Figure 9 – DER-1035Q Mid-Layer 2 PCB Layout.

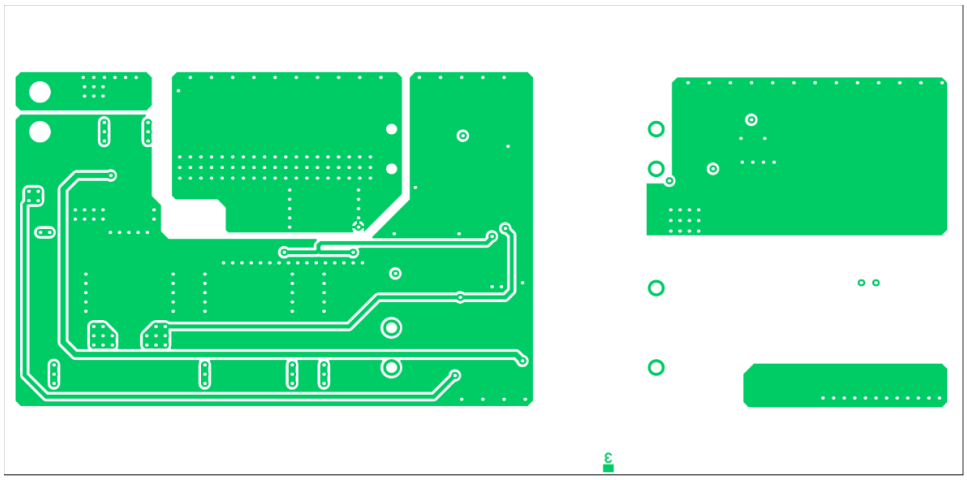


Figure 10 – DER-1035Q Mid-Layer 3 PCB Layout.

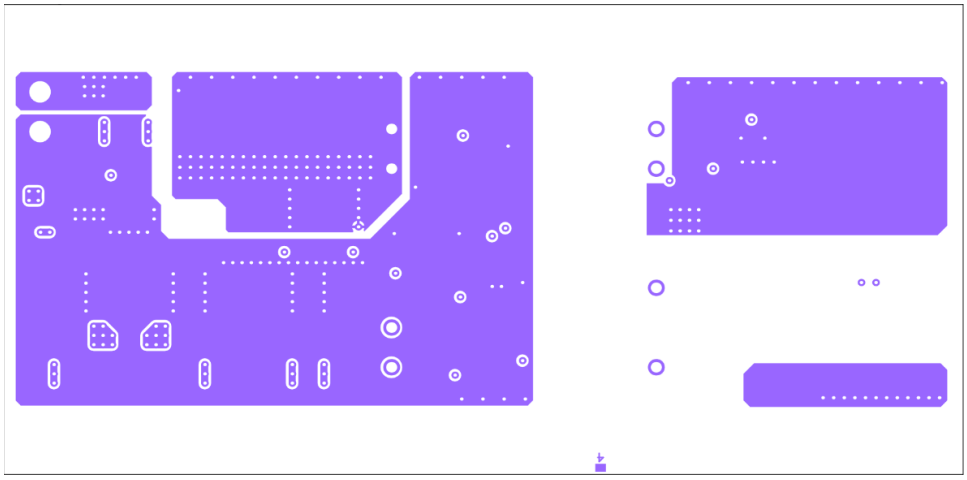


Figure 11 – DER-1035Q Mid-Layer 4 PCB Layout.

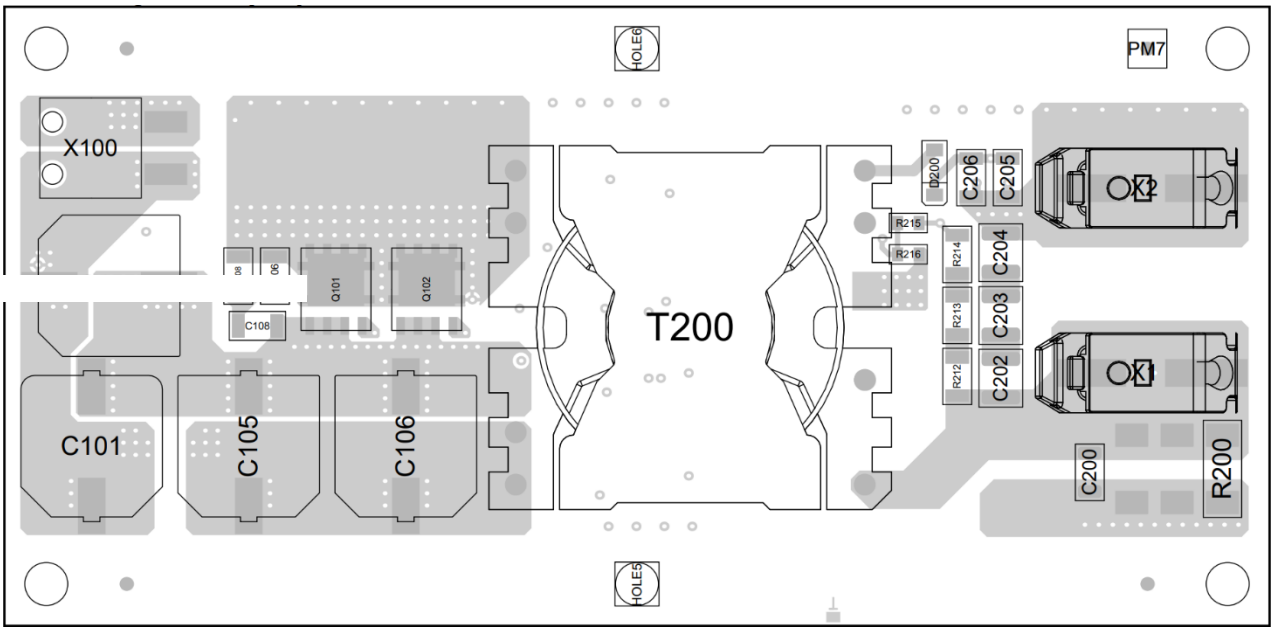


Figure 12 – DER-1035Q PCB Assembly (Top).

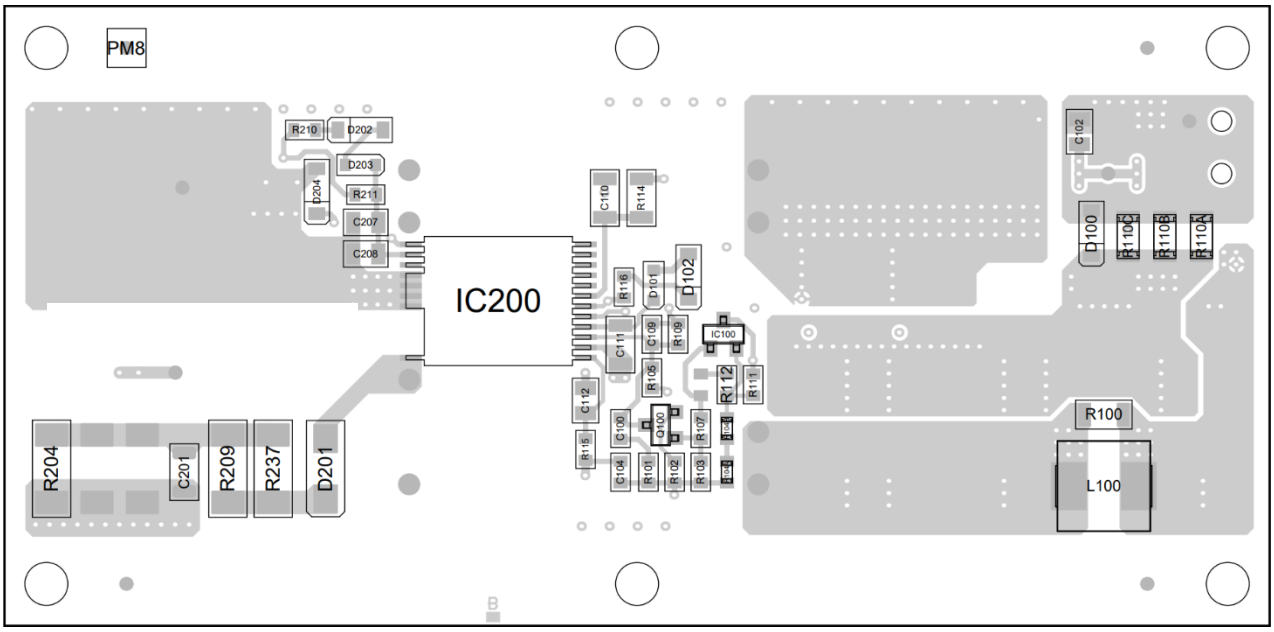


Figure 13 – DER-1035Q PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 47 nF X7R/50 V/10% 0603	C0603C103K5RACAUTO7411	KEMET
2	1	C101	Polymer Aluminium Capacitor 1000 µF AL/25 V/20% 10.3X10.3mm	EEH-ZS1E102UP	Panasonic
3	1	C102	Ceramic Chip Capacitor 2.2 µF X7R/35 V/10% 0805	CGA4J1X7R1V225K125AC	TDK
4	1	C103	Ceramic Chip Capacitor 10 nF X7R/50 V/10% 0603	C0603C103M5RACAUTO	KEMET
5	1	C104	Ceramic Chip Capacitor 100 nF X7R/50 V/10% 0603	CGA3E2X7R1H104K080AA	TDK
6	3	C105, C106, C107	Polymer Aluminium Capacitor 560 µF AL/25 V/20% 10.3X10.3mm	EEH-ZU1E561P	Panasonic
7	1	C108	Ceramic Chip Capacitor 2.2 nF C0G/630 V/5% 1206	GCM31B5C2J222JX01L	Murata
8	1	C109	Ceramic Chip Capacitor 330 pF C0G/50 V/5% 0603	GCM1885C1H331JA16D	Murata
9	1	C110	Ceramic Chip Capacitor 330 pF C0G/630 V/5% 1206	CGA5C4C0G2J331J060AA	TDK
10	1	C111	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 1206	GCM31CR71H225KA55K	Murata
11	1	C112	Ceramic Chip Capacitor 1 µF X7R/50 V/10% 0805	CGA4J3X7R1H105K125AB	TDK
12	2	C200, C201	Ceramic Chip Capacitor 1500 pF C0G/630 V/5% 1206	CGA5H4C0G2J152J115AA	TDK
13	3	C202, C203, C204	Ceramic Chip Capacitor 150 nF X7R/500 V/10% 1210	C1210X154KCRACAUTO	KEMET
14	2	C205, C206	Ceramic Chip Capacitor 10 µF X7R/50 V/10% 1206	CGA5L1X7R1H106K160AC	TDK
15	2	C207, C208	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 0805	CGA4J3X7R1H225K125AE	TDK
16	1	D100	Schottky Diode PMEG4030ER/8X 40 V/3A SOD123W	PMEG4030ER/8X	Nexperia
17	2	D101, D203	Diode Schottky 40 V 350 mA SD103AWS-AU 40 V / 350mA SOD-323	SD103AWS-AU_R1_000A1	Panjit
18	1	D102	Zener Diode 9.1 V 500 mW ±5% SMT SOD-123 MMSZ5239B-7-F 9.1V SOD-123	MMSZ5239B-7-F	Diodes, Inc.
19	1	D200	Diode Standard 200 V 225 mA (DC) SMT SOD-123 BAS21GWX 200 V / 225mA SOD-123	BAS21GWX	Nexperia
20	1	D201	DIODE SCHOTTKY 1 kV 1 A ACURA107 1000 V / 1A DO-214AC (SMA)	ACURA107-HF	Comchip
21	1	D202	DIODE ZENER 24 V 500 mW SOD123 BZT52C24-7-F 24V SOD-123	BZT52C24-7-F	Diodes, Inc.
22	1	D204	not assembled Diode N.A. SOD123	N.A.	N.A.
23	1	IC100	Voltage References Automotive, high-bandwidth, low-IQ programmable shunt regulator ATL431LIBQDBZRQ1 2.5 V to 36 V SOT-23	ATL431LIBQDBZRQ1	Texas Instruments
24	1	IC200	InnoSwitch3-AQ 4.65 V to 5.15 V/Vmos=1700 V InSOP-24D	INN3949CQ	Power Integrations
25	1	L100	Shielded Power Inductor 220 nH 7.00 mm x 6.60 mm	SRP7028TA-R22Y	Bourns
26	1	Q100	40 V / 0.2 A PNP bipolar transistor MMBT3906-7-F PNP/40V/0.2A/300mW SOT-23	MMBT3906-7-F	Diodes, Inc.
27	2	Q101, Q102	N-Channel MOSFET DMT15H017LPS-13 150 V 9.4 A (Ta), 58A (Tc) 1.3W (Ta) PowerDI5060-8	DMT15H017LPS-13	Diodes, Inc.
28	1	R100	Thick Film Chip Resistor N.A. 1%/0.25W/200V 1206	N.A.	N.A.
29	2	R101, R109	Thick Film Chip Resistor 10 kΩ 5%/0.1W/75 V 0603	AC0603JR-0710KL	YAGEO
30	1	R102	Thick Film Chip Resistor 430 kΩ 5%/0.1W/150 V 0603	ERJ-3GEYJ434V	Panasonic
31	1	R103	Thick Film Chip Resistor 33 kΩ 5%/0.1W/150 V 0603	RMCF0603JT33K0	Stackpole
32	1	R104A	Thick Film Chip Resistor 91 kΩ 1%/0.1W/150 V 0603	RK73H1JTTD9102F	KOA Speer
33	2	R104B, R112	Thick Film Chip Resistor 1 kΩ 5%/0.1W/75 V 0603	CRGCQ0603J1K0	TE Connectivity
34	1	R105	Thick Film Chip Resistor 110 kΩ 5%/0.1W/150 V 0603	RMCF0603JT110K	Stackpole
35	2	R106, R108	Thick Film Chip Resistor 27 Ω 5%/0.5W/500 V 1206	SR1206FR-7W27RL	YAGEO
36	1	R107	Thick Film Chip Resistor 11 kΩ 5%/0.1W/150 V 0603	RMCF0603JT11K0	Stackpole
37	2	R110A, R110B, R110C	Current Sense Resistor 0.018kΩ 1%/ ½ W /200 V 1206	UCR18EVHFSR018	Rohm Semi
38	1	R111	Thick Film Chip Resistor 20 kΩ 1%/0.1W/75 V 0603	ERJ-3EKF2002V	Panasonic
39	1	R114	Thick Film Chip Resistor 100 Ω 5%/0.25W/200 V 1206	RMCF1206JT100R	Stackpole
40	1	R115	Thick Film Chip Resistor 10 Ω 5%/0.1W/75 V 0603	CRGCQ0603J10R	TE Connectivity
41	2	R116, R210	Thick Film Chip Resistor 75 Ω 1%/0.1W/150 V 0603	AC0603FR-0775RL	YAGEO

42	2	R200, R204	MELF Resistors 390 kΩ 1%/1W/350 V MELF 0207	MMB02070C3903FB200	Vishay
43	6	R201, R202, R205, R206, R209, R237	MELF Resistors N.A. 1%/1 W/200 V MELF 0207	N.A.	N.A.
44	1	R211	Thick Film Chip Resistor 2 kΩ 1%/0.1 W/75 V 0603	RMCF0603FT2K00	Stackpole
45	3	R212, R213, R214	Thick Film Chip Resistor N.A. 1206	N.A.	N.A.
46	1	R215	Thick Film Chip Resistor N.A. 0603	N.A.	N.A.
47	1	R216	Thick Film Chip Resistor 0R 0603	RMCF0603ZT0R00	Stackpole
48	1	T200	PQ2620_THT PQ2620	PQ2620	Power Integrations
49	1	X1	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN04G7 RED	SM99S01VBNN04G7	METZ CONNECT
50	1	X100	TERMI-BLOK SMD MOUNT 180_2P_3.81 2383945-2 12A 1x2Pin,Pitch 3.81mm	2383945-2	TE
51	1	X2	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN00G7 BLACK	SM99S01VBNN00G7	METZ CONNECT
52	1	Z1	Printed Circuit Board PCB 1.55 mm PCB thickness 1.55 mm N		

Table 4 – DER-1035Q Bill of Materials[9].

[9] All components are AEC-Q qualified except the SR MOSFET, connectors, and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

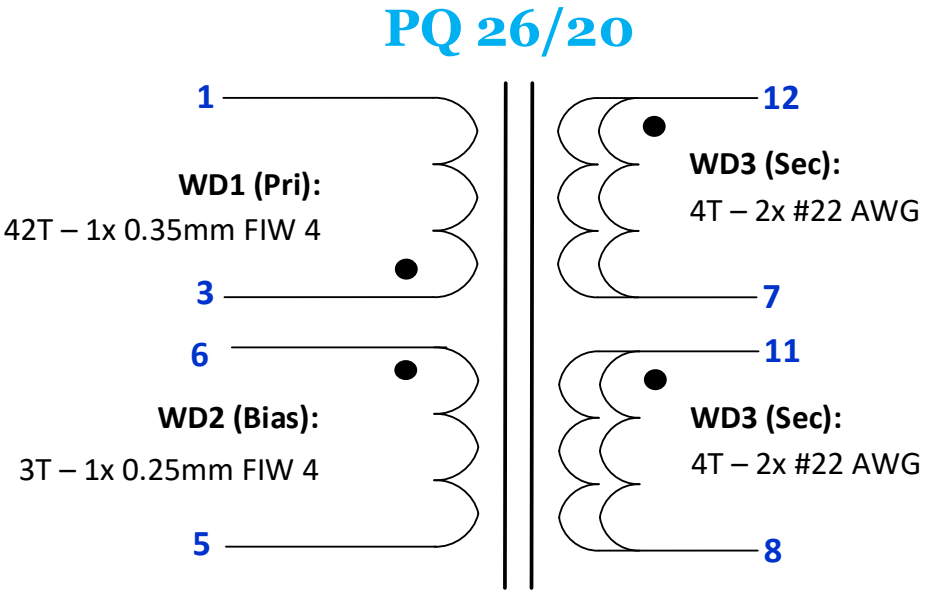


Figure 14 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			70	W
Input voltage Vdc	Flyback topology	190	300	450	V
Switching frequency	Flyback topology			60	kHz
Duty cycle	Flyback topology	16.5		43.7	%
Np:Ns			11		
Rdc	Primary side		454		mΩ
Rdc	Secondary side		12		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency between pin 3 and pin 7, with pins 5-6 shorted, pins 1-3 shorted and pins 7-8-11-12 shorted at 25°C		55.4		pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		779.5		µH
Part to part tolerance	Tolerance of Primary Inductance		5		%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.		6.16		µH

Table 5 – Transformer (T1) Electrical Specifications.

7.3 Transformer Build Diagram

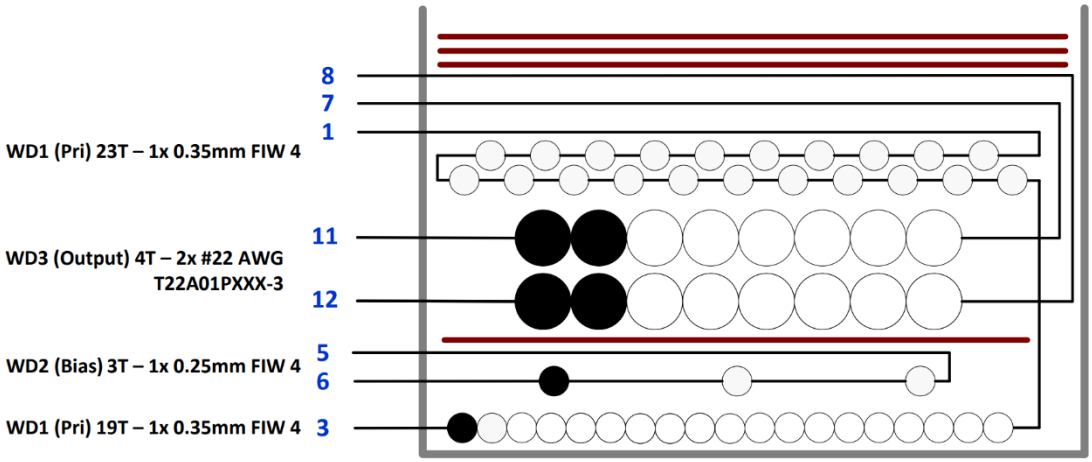


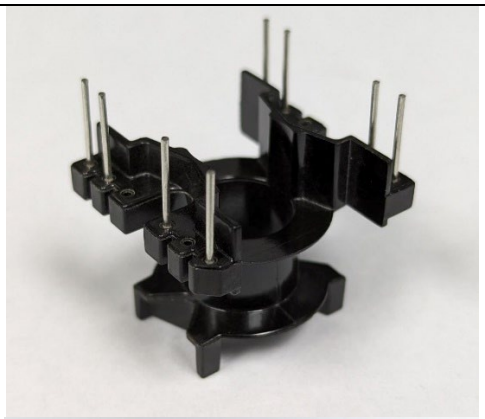
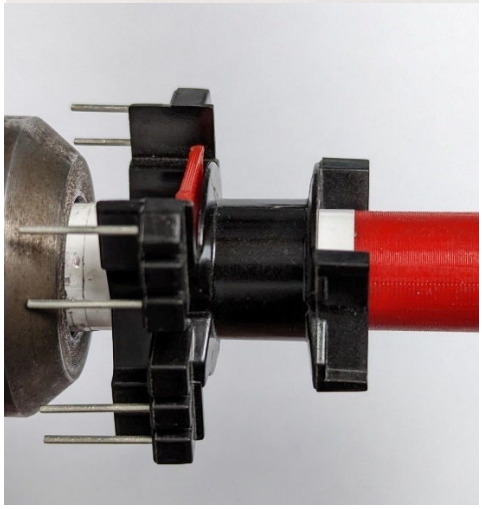
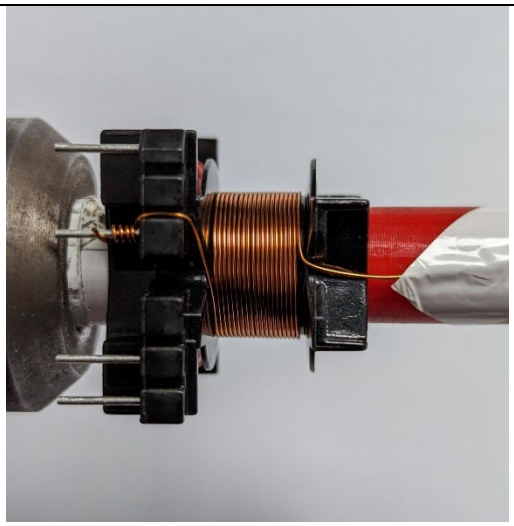
Figure 15 – Transformer Build Diagram.

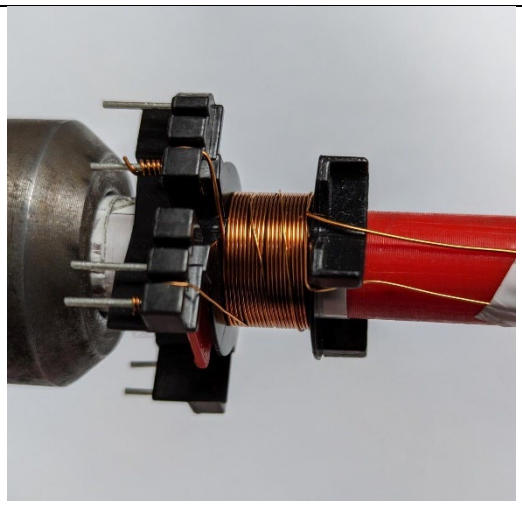
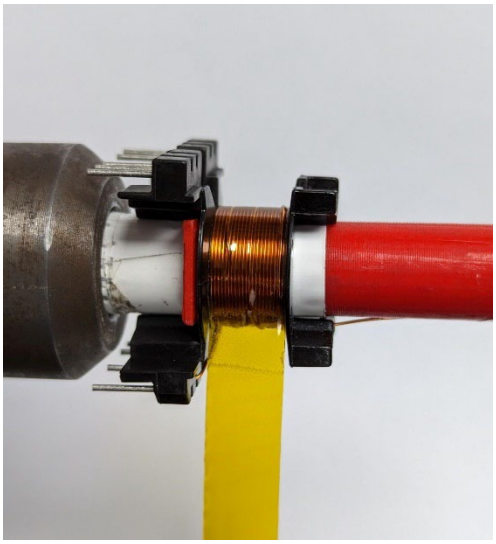
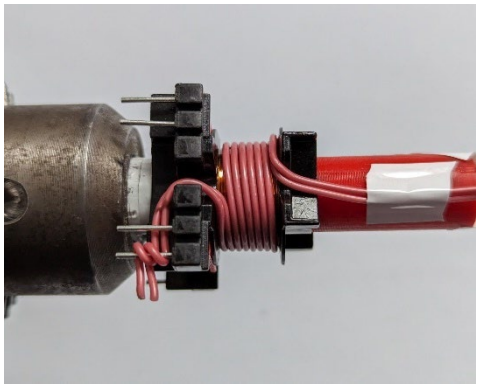
7.4 Material List

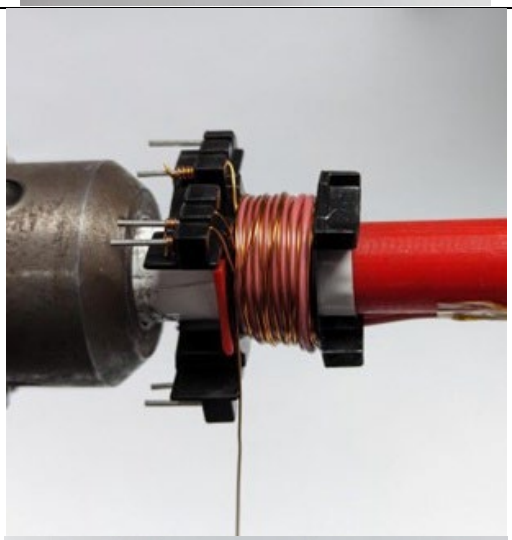
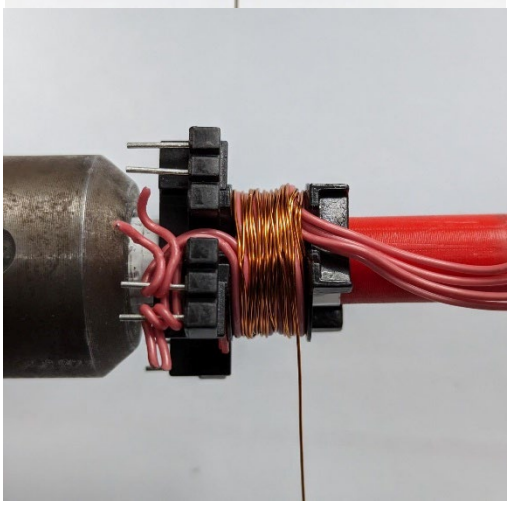
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: PQ26/20 – 2 (P6-S6)	1	PC	Phenolic	FerroxCube
[2]	Core: PQ26	2	PCS	PC95 (or equivalent)	TDK
[3]	WD1 (Pri): 0.35mm FIW 4, Class F		mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.25mm FIW 4, Class F		mm		Elektrisola
[5]	WD3 (VOUT): AWG 22 PFA 0.003”		mm		Rubadue
[5]	3M Polyimide Film Tape 5413, width: 0.38in (9.65mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

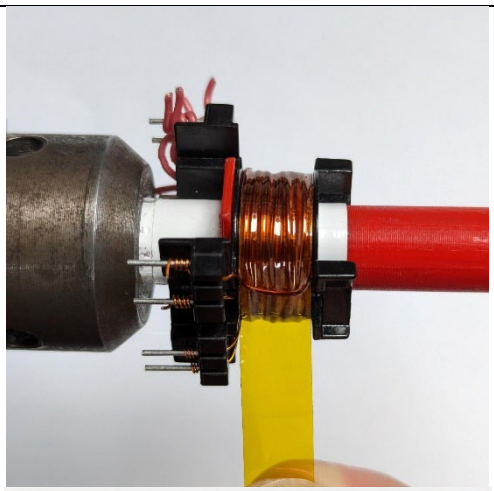
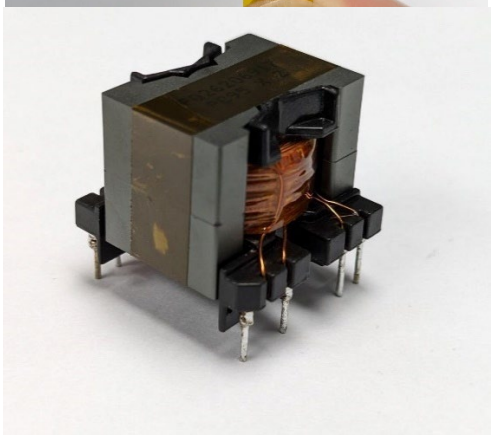
Table 6 – Transformer (T200) Material List.

7.5 Winding Instructions

Winding Preparation	 	Start by removing the unused pins 2, 4, 5 and 10 of the bobbin. Position the bobbin on the mandrel such that the pins of the bobbin is on the left side. Winding direction is clockwise direction.
WD1 (Pri)		Use 0.35mm FIW4 wire. Start on PIN 3. Wind the primary winding's first layer, 19 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

WD2 (Bias)	 	Use 0.25mm FIW4 wire. Start on PIN 6. Wind the bias winding, 3 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Terminate bias winding at PIN 5. Secure using 1 Layer of tape.
WD3 (VOUT)		Use 2 x 22 AWG wire. Start on PIN 12. Wind the secondary winding's first layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

		Use 2 x 22 AWG TIW wire. Start on PIN 11. Wind the secondary winding's first layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD1 (Pri)	 	Continue winding the primary wire. Wind the primary winding's second layer, 12 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Continue winding the primary wire. Wind the primary winding's third layer, 11 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

Finishing	 	Terminate primary winding at PIN 1. Terminate secondary winding at PIN 7 and 8. Secure using 3 Layers of tape. Mount the gapped core using glue (a polyester film electrical tape can be used as alternative)

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	14.00		14.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	190.00		190.00	V	Input DC voltage 1
6	IOUT1	5.00		5.000	A	Output current 1
7	POUT1			70.00	W	Output power 1
8	EFFICIENCY1	0.85		0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	450.00		450.00	V	Input DC voltage 2
13	IOUT2	5.00		5.00	A	Output current 2
14	POUT2			70.00	W	Output power 2
15	EFFICIENCY2	0.85		0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.981	A	Primary switch minimum current limit
78	ILIMIT_TYP			2.130	A	Primary switch typical current limit
79	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.44	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			602	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	60000		60000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	147.0		147.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			0.995		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			CCM		Mode of operation

90	DUTYCYCLE			0.437		Primary switch duty cycle
91	TIME_ON_MIN			3.22	us	Minimum primary switch on-time
92	TIME_ON_MAX		Info	8.69	us	Maximum primary switch on-time is greater than 11.75us: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			9.45	us	Primary switch off-time
94	LPRIMARY_MIN			737.8	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			776.6	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			815.4	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.402	A	Primary switch average current
101	IPEAK_PRIMARY			2.053	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.009	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			2.053	A	Primary switch ripple current
104	IRMS_PRIMARY			0.742	A	Primary switch RMS current
108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	PQ26		PQ26		Core selection
111	CORE NAME			PQ26/20-PC95		
112	AE			121.0	mm^2	Core cross sectional area
113	LE			45.0	mm	Core magnetic path length
114	AL			5530	nH	Ungapped core effective inductance per turns squared
115	VE			5470	mm^3	Core volume
116	BOBBIN NAME			PQ26/20 - 2 (P6-S6)		Bobbin name
117	AW			31.1	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			9.00	mm	Bobbin width
119	BH			4.78	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122	**PRIMARY WINDING**					
123	NPRIMARY			42		Primary winding number of turns
124	BPEAK			3743	Gauss	Peak flux density
125	BMAX			3243	Gauss	Maximum flux density
126	BAC			1621	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			440	nH	Typical gapped core effective inductance per turns squared
128	LG			0.318	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	4		4		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			3		Bias winding number of turns

138	**PRIMARY COMPONENTS SELECTION**					
161	**BIAS WINDING**					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			39.36	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	uF	Bias winding rectification capacitor
166	CBPP			4.70	uF	BPP pin capacitor
170	**SECONDARY COMPONENTS SELECTION**					
171	**FEEDBACK COMPONENTS**					
172	RFB_UPPER[10]			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			10.00	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	**MULTIPLE OUTPUT PARAMETERS**					
179	OUTPUT 1					
180	VOUT1			14.00	V	Output 1 voltage
181	IOUT1			5.000	A	Output 1 current
182	POUT1			70.00	W	Output 1 power
183	IRMS_SECONDARY1			8.843	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			7.293	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			4		Number of turns for output 1
186	VREVERSE_RECTIFIER1			54.48	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT15H017LPS-13		DMT15H017LPS-13		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
218	PO_TOTAL			70.00	W	Total power of all outputs

Table 7 – DER-953Q PIXls Spreadsheet.

[10] Actual value implemented on the unit is 110 kΩ as requirement for implementing the *Precision Voltage Regulator* circuit.

9 Performance data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a high-voltage (HV) room.

Figure 16 – High-Voltage Test Set-up.

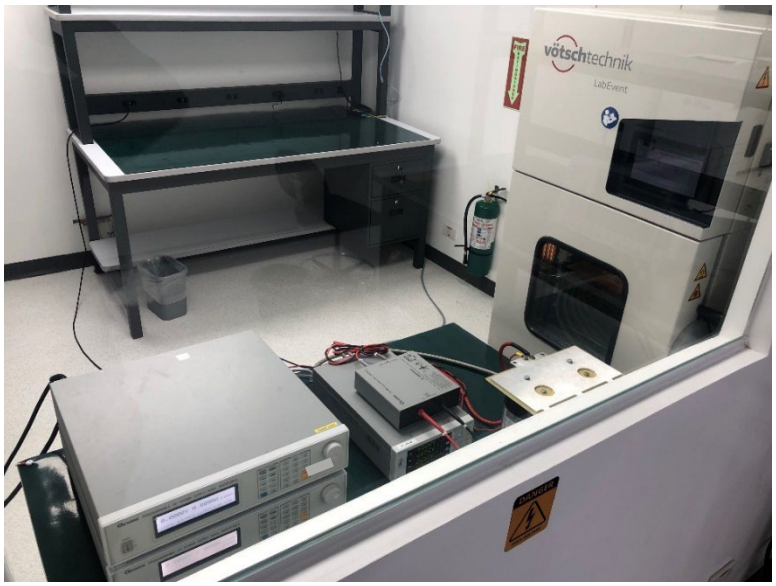


Figure 17 – Test Set-up Inside the High-Voltage Room.

2. Unit under test was placed under a box inside the thermal chamber to eliminate the effects of any airflows.

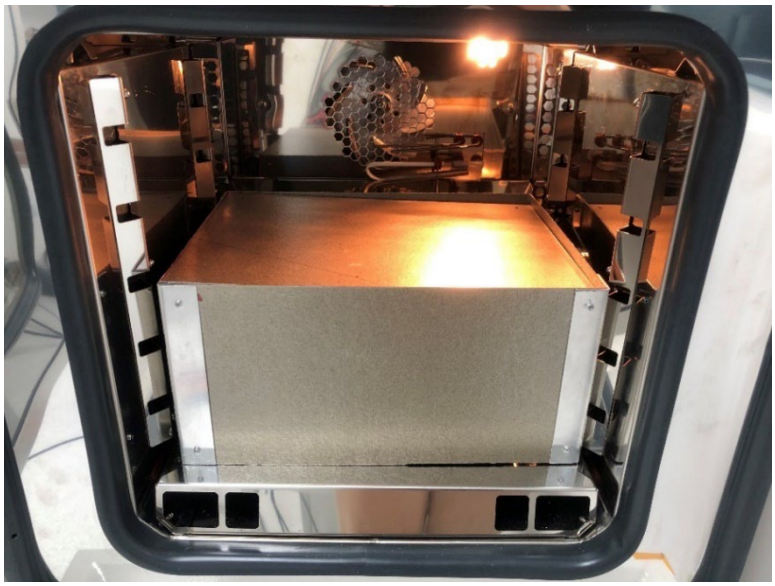


Figure 18 – Unit Under Test Placed Under a Box to Eliminate the Effect of Airflow.

3. Unit under test was soaked for 5 minutes at full load condition with every change in the input voltage during the start of every test sequence. The unit under test was soaked for at least 1 min for every loading condition before measurements were taken.
4. The following data were taken without CMC
5. List of Equipment Used for Testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	62024P-600-8	600 V / 8 A / 2400 W DC PSU	Chroma
Electronic Load	DL3021	150 V / 40 A / 200 W DC ELOAD	Rigol
Electronic Load	PEL-2020A	80 V / 20 A / 100 W DC ELOAD	GW Instek
Power Meter	66205	600 V / 30 A 10 kHz Digital Meter	Chroma
Power Meter	WT310E	600 V/20 A 100 kHz Digital Meter	Yokogawa
Current Meter	DMM-4050	Precision Multimeter	Tektronix
High Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Output Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Component Current Measurement	CWTUM/015/B	30 MHz 30 A_{peak} Rogowski Coil	CWT
Component Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20 channel Data Logger	Graphtec
Thermal Image	TiX580	1000°C Thermal Imagin Camera	Fluke
Oscilloscope	DLM5058	2.5GS/s 500 MHz Mixed Signal	Yokogawa
Power Supply	62024P-600-8	600 V / 8 A / 2400 W DC PSU	Chroma

Table 8 – List of Equipment Used for Testing.

9.1 No-Load Input Power

Figure 19 shows the test set-up diagram for no-load input current acquisition. The voltage measuring point is placed before the ammeter; this is done to prevent the voltage-sensing bias current from affecting the input current measurement. The ammeter used was a Tektronix DMM 4050 6-1/2 Digit Precision Multimeter.

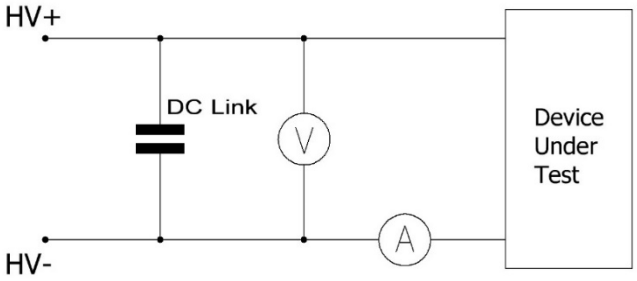


Figure 19 – No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes for every change in input voltage before starting data averaging over five minutes. Analog filtering is also enabled to improve measurement accuracy.

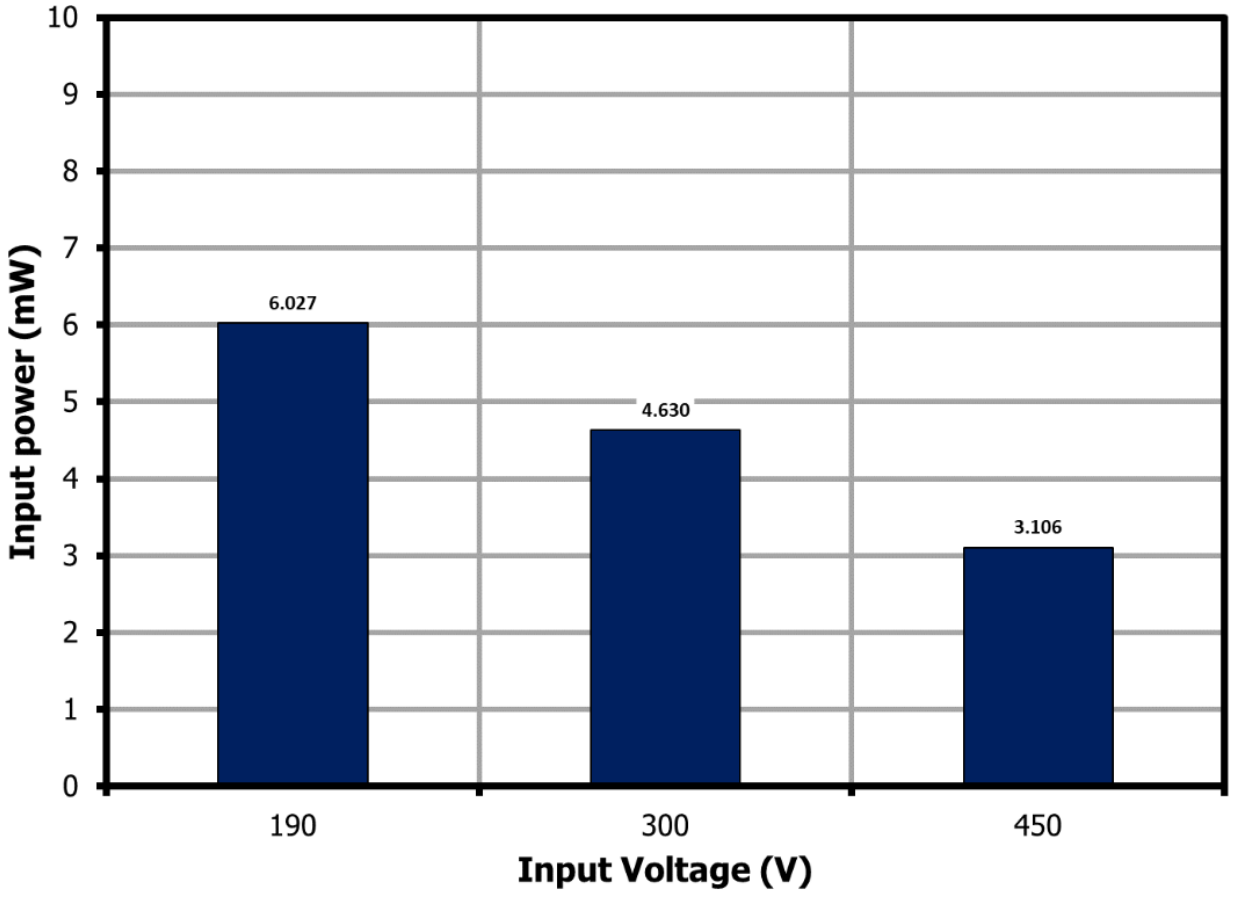


Figure 20 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Line Efficiency

Line efficiency describes how the input voltage change affects the unit's overall efficiency. The points in the graph are only taken from 100% load conditions.

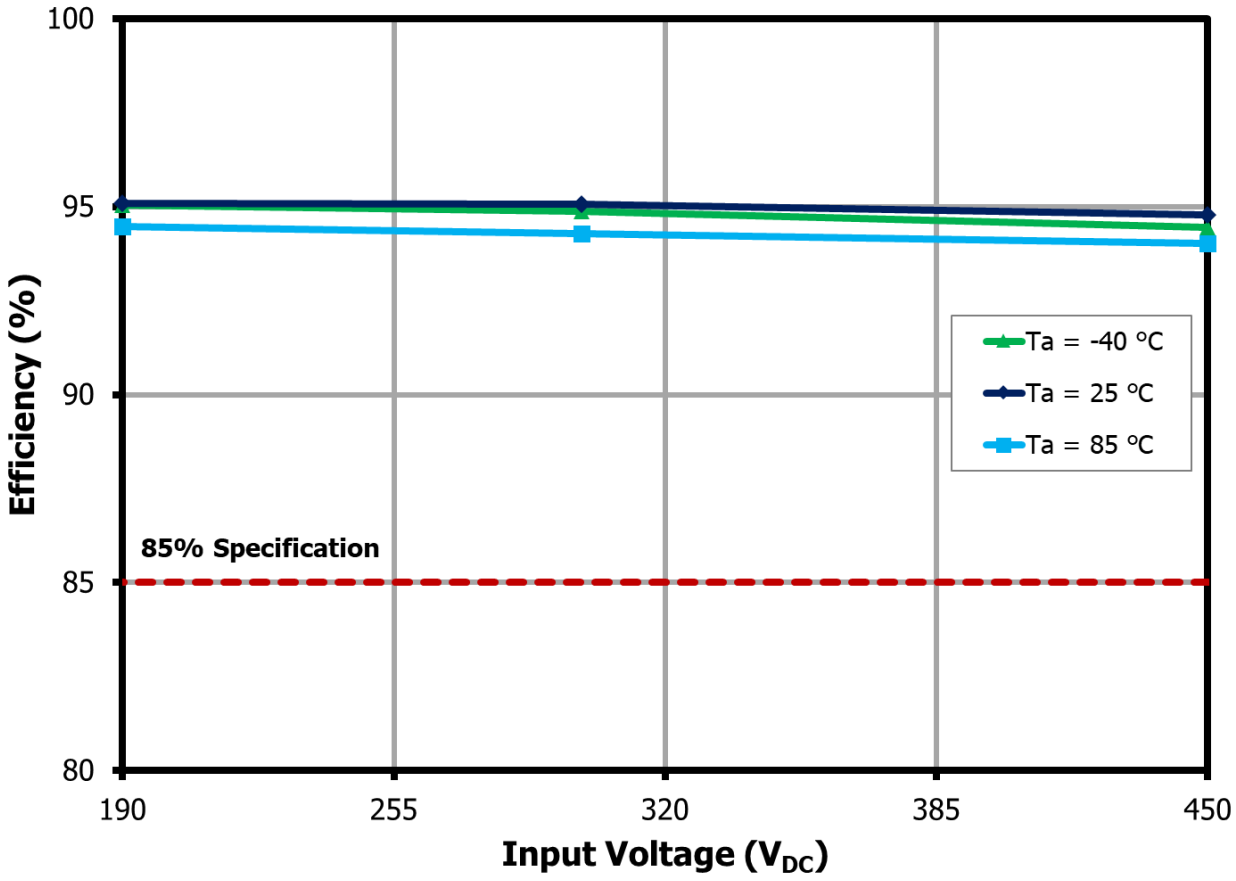


Figure 21 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the unit's overall efficiency.

9.2.2.1 Load Efficiency at 85 °C

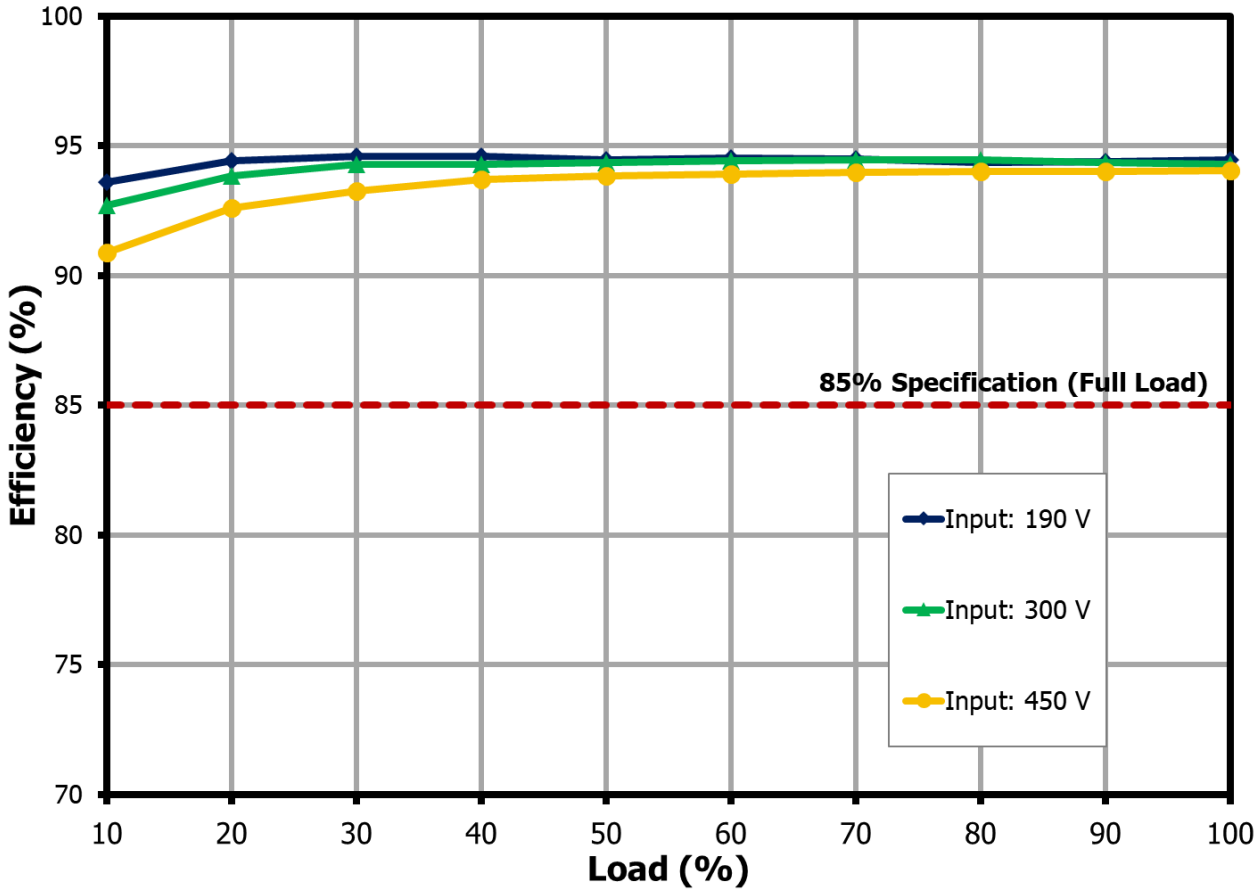


Figure 22 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

9.2.2.2 Load Efficiency at -40 °C

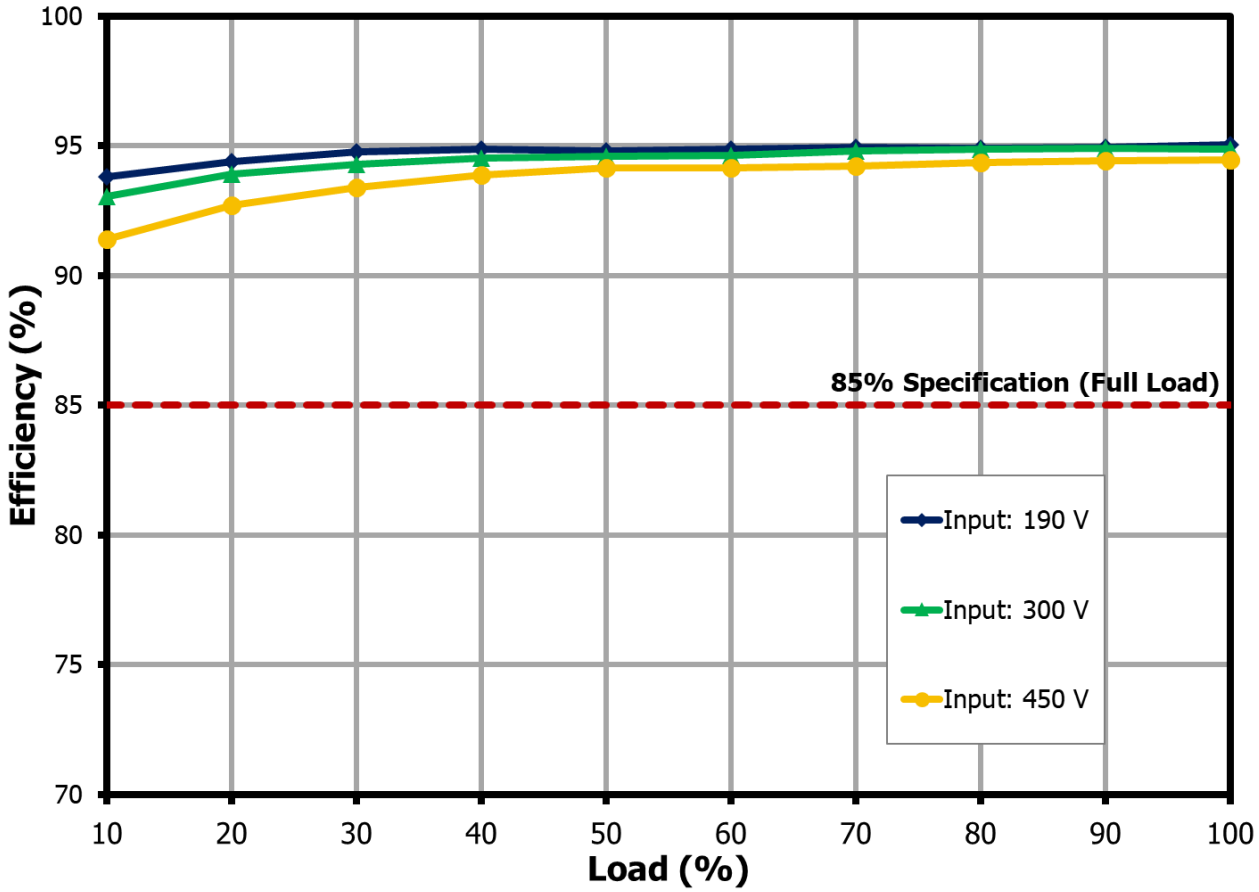


Figure 23 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.2.2.3 Load Efficiency at 25 °C

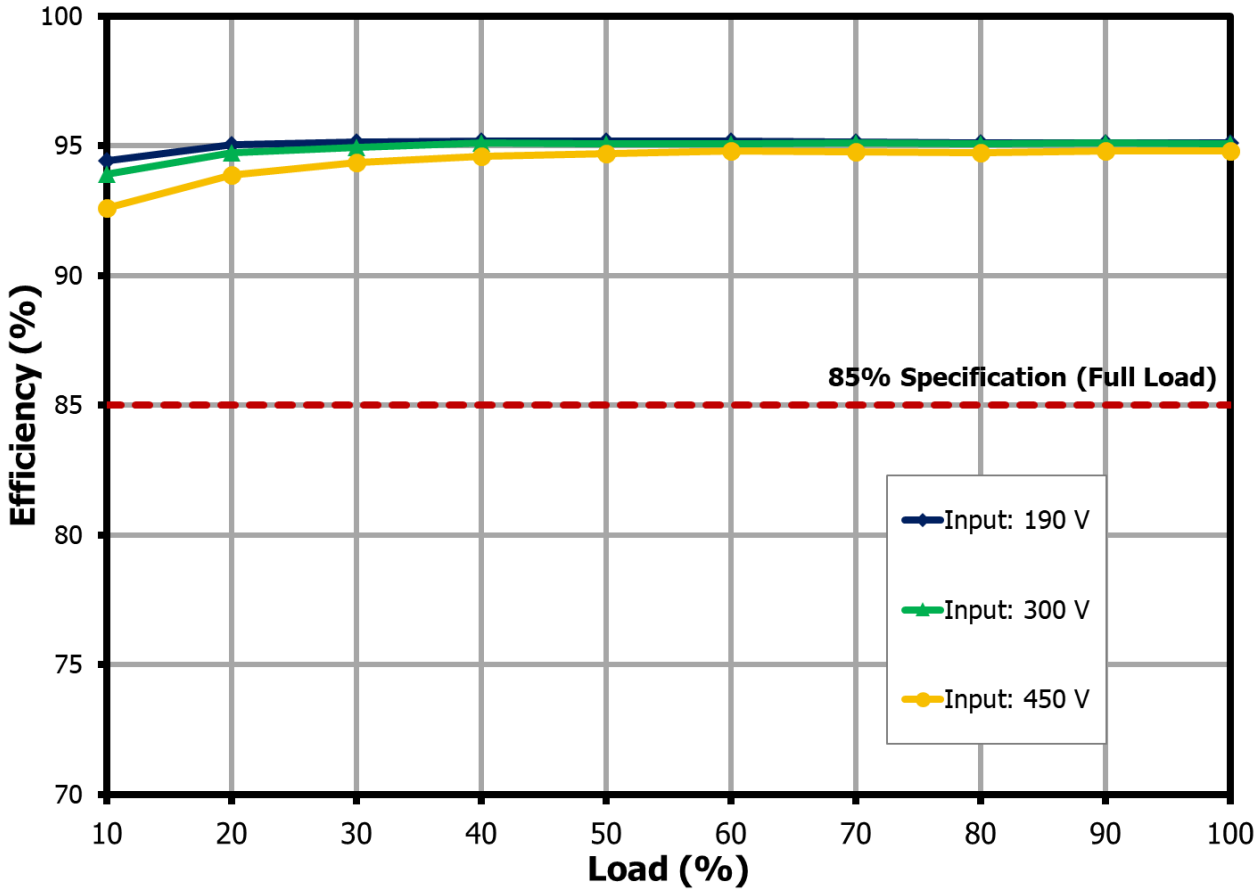


Figure 24 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.3 Output Line and Load Regulation

9.3.1 Load Regulation

Load Regulation describes how the change in output loading conditions affects the average output voltage of the unit.

9.3.1.1 Load Regulation at 85 °C

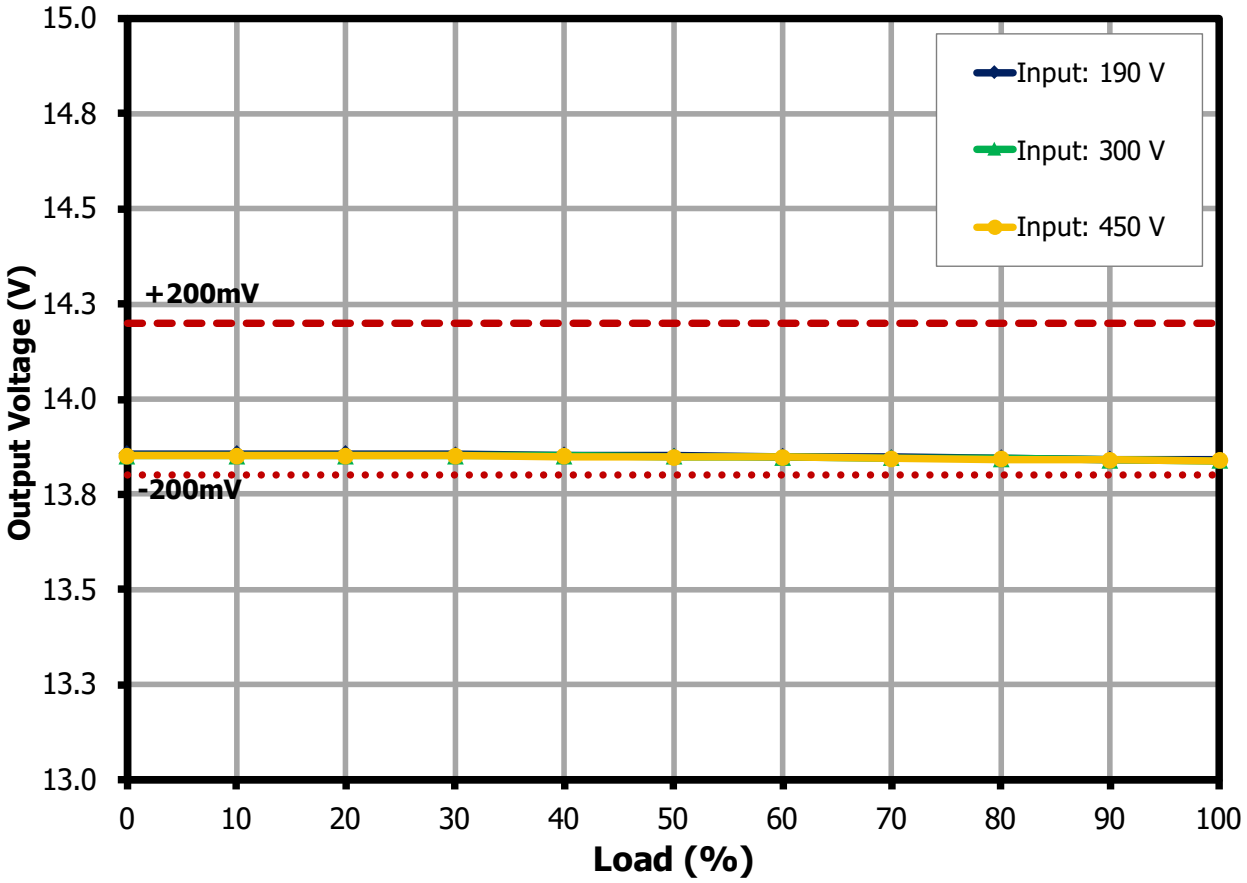


Figure 25 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at -40 °C

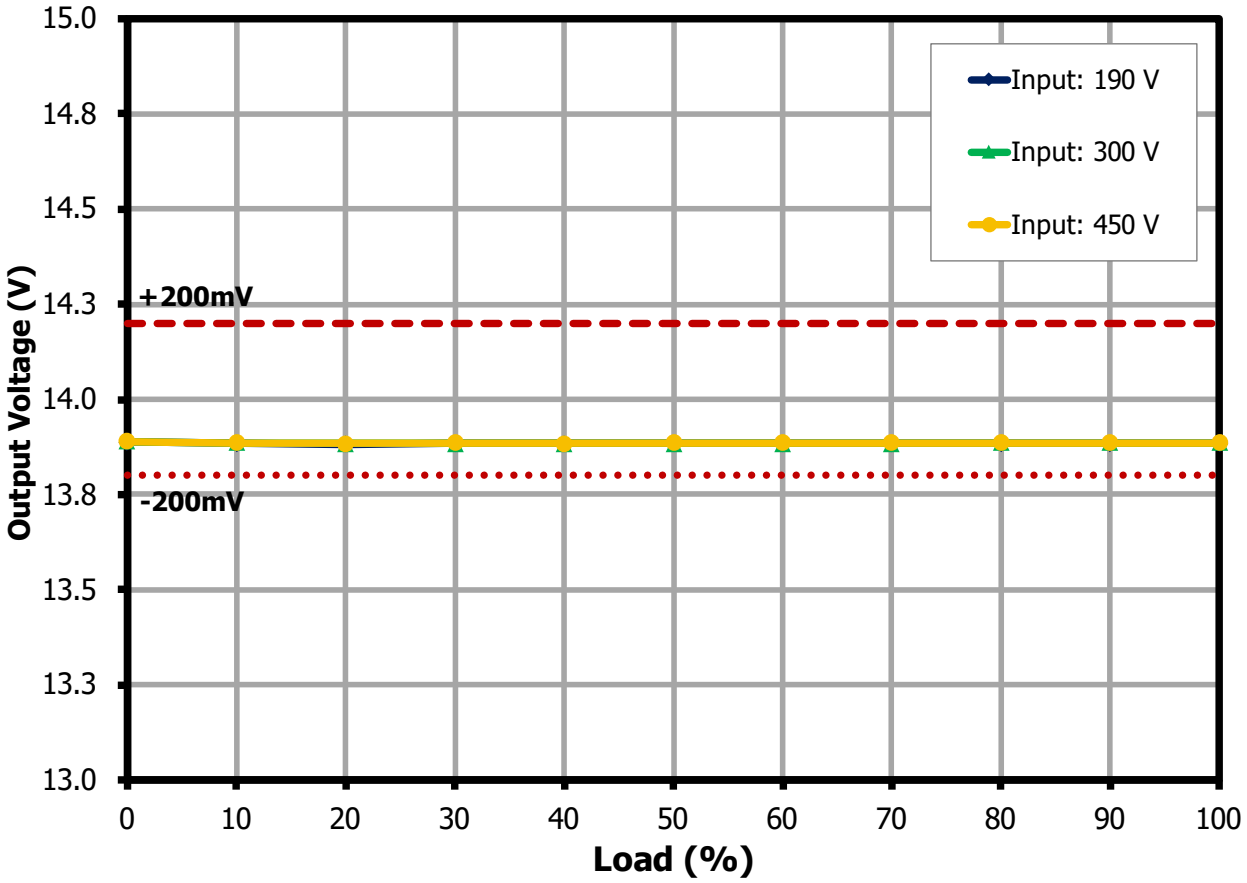


Figure 26 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.1.3 Load Regulation at 25 °C

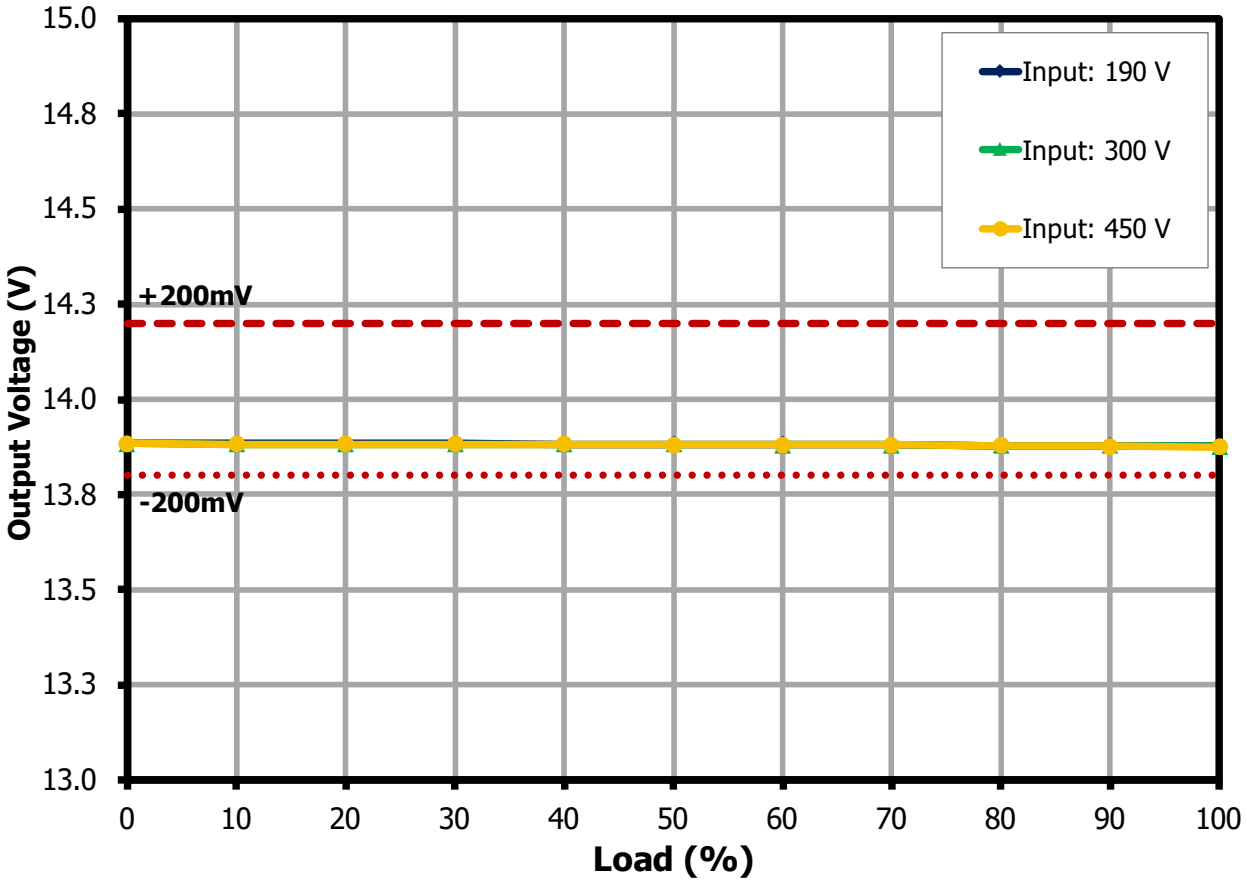


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.2 Line Regulation

Line Regulation describes how the change in input voltage conditions affects the average output voltage of the unit. The points in the following graph are only taken from 100% load conditions.

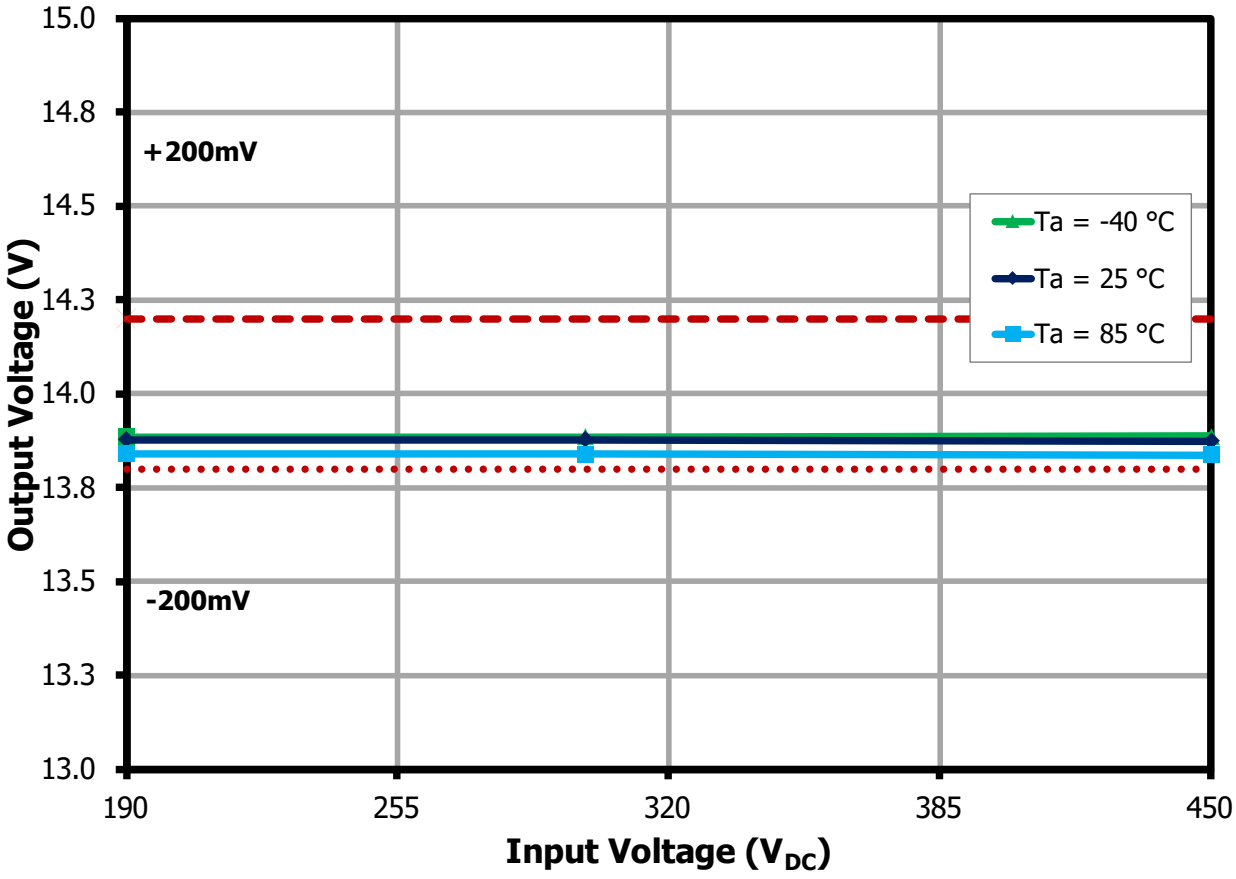


Figure 28 – Output Voltage vs Input Voltage at Full Load.

10 Thermal Performance

10.1 Thermal Data at 85 °C

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 18 shows the set-up for thermal measurement.

Critical Components	Input Voltage		
	190	300	450
InnoSwitch3- AQ (IC200A)	117.15	109.9	112.45
Primary Snubber Resistor (R204)	100.1	96.55	99.4
Primary Snubber Diode (D201)	102.9	100.25	101.8
Transformer Core	112.85	110.9	113.1
Transformer Winding	116.75	106.25	113.6
Output Capacitor (C106)	113.25	109.3	110.35
Synchronous Rectifier MOSFET (Q102)	124.3	118.1	119.75
Secondary Snubber Resistor (R106)	125.3	119.5	108.5
Output Current Sense Resistor (R110A)	112.1	106.15	108.5

Table 9 – Thermal Data at 85 °C at Different Input Voltages (°C).

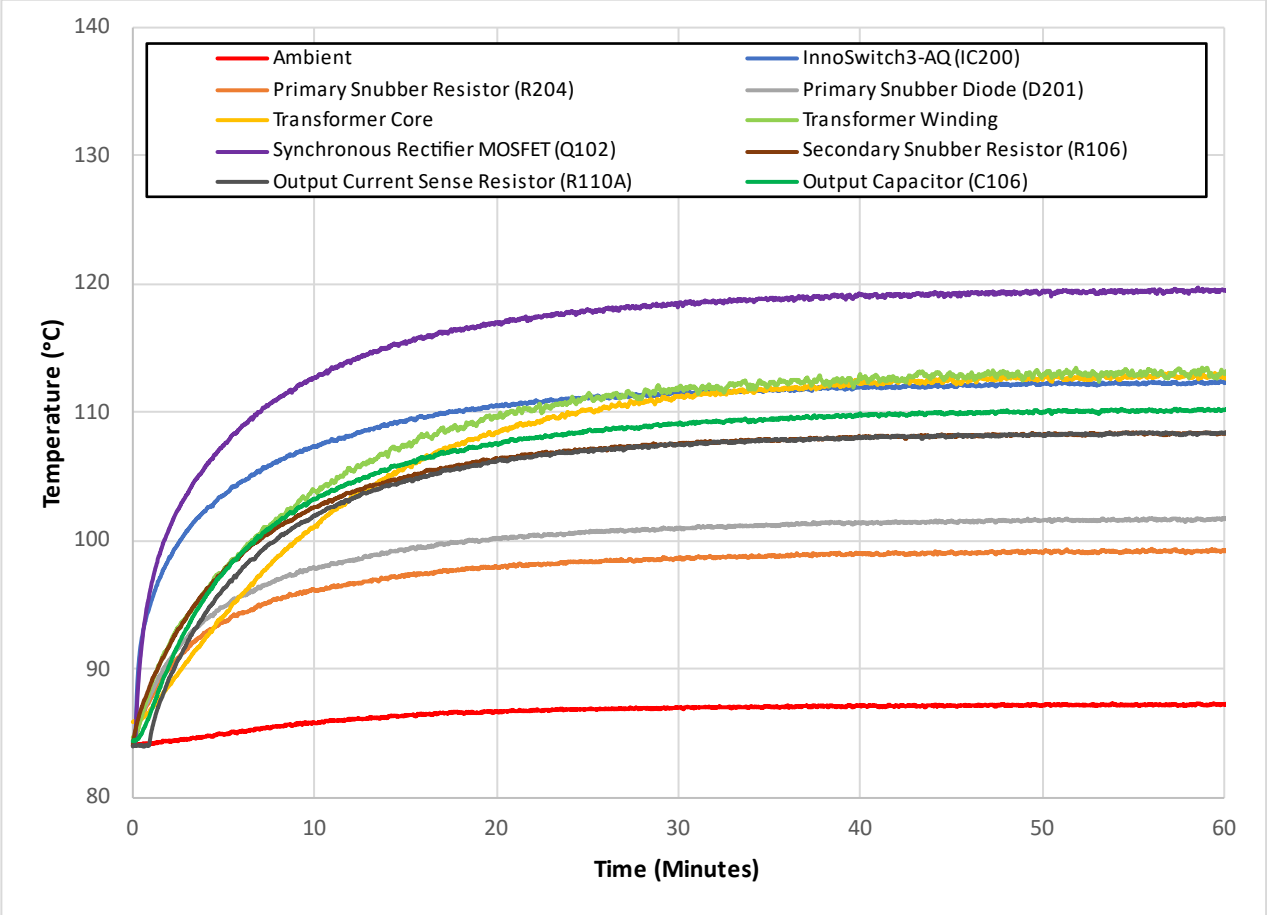


Figure 29 – Component Temperatures at 85 °C Ambient, 450 V Input.

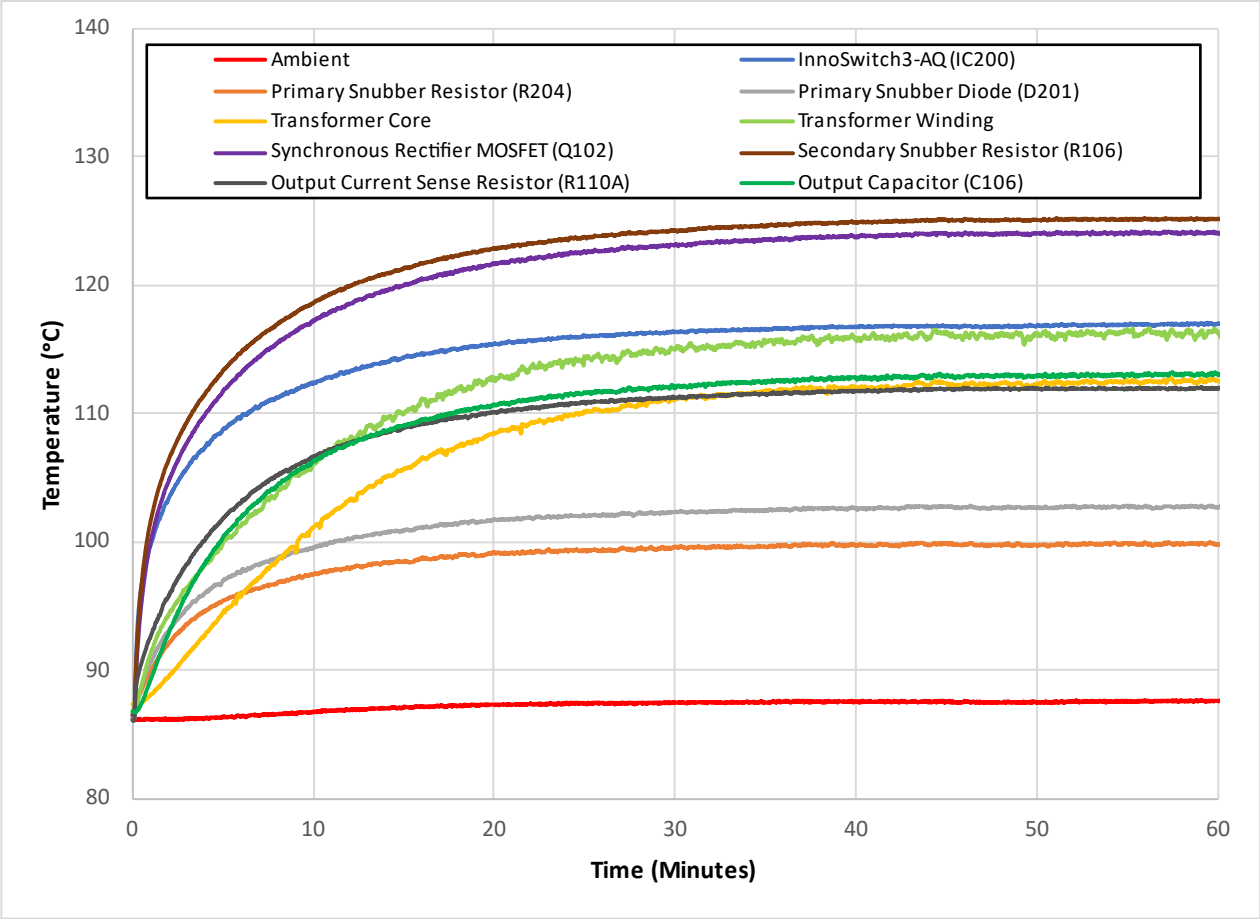


Figure 30 – Component Temperatures at 85 °C Ambient, 190 V Input.

10.2 Thermal Image Data at 25 °C

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour. The set-up is inside an enclosure to minimize the effect of airflow.

Critical Components	Input Voltage		
	190 V	300 V	450 V
InnoSwitch3- AQ (IC200A)	55.1	51.1	59.1
Primary Snubber Resistor (R204)	36.7	39.4	38.1
Primary Snubber Diode (D201)	41	40.8	42.4
Transformer Core	54.4	56.1	56.6
Transformer Winding	60.3	61.9	62.5
Output Capacitor (C106)	48.6	50.6	50.8
Synchronous Rectifier MOSFET (Q102)	54.5	57.4	58.5
Secondary Snubber Resistor (R106)	52.3	57.9	62.4
Output Current Sense Resistor (R110A)	49.6	51	49.9

Table 10 – Thermal Data at 25 °C at Different Input Voltages (°C).

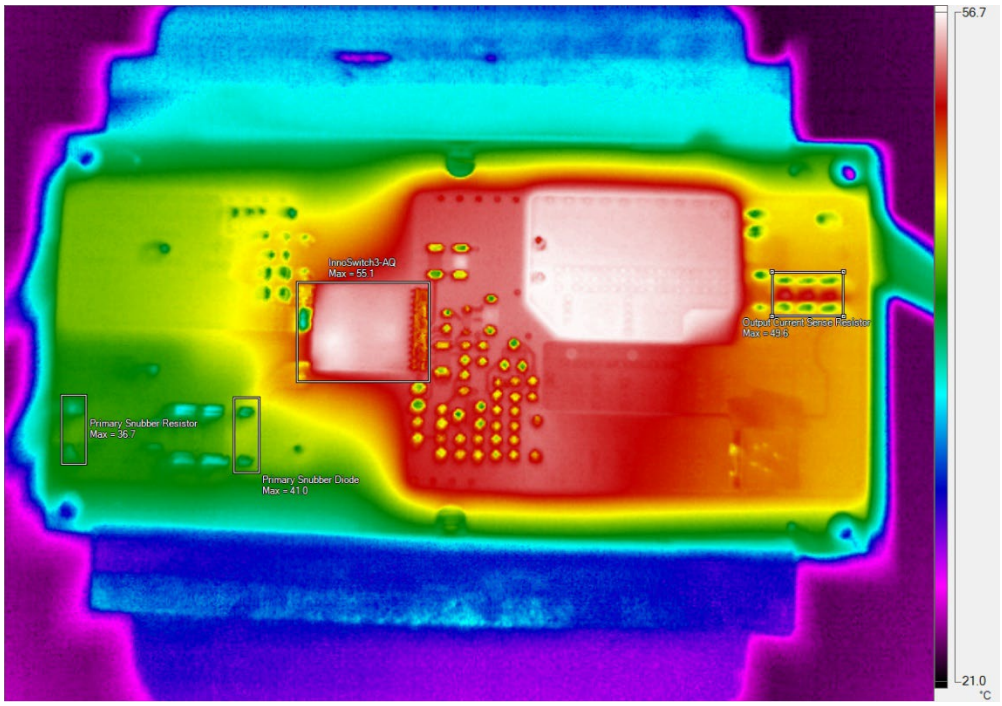


Figure 31 – PCB Bottom Thermal Scan at 190 V Input.

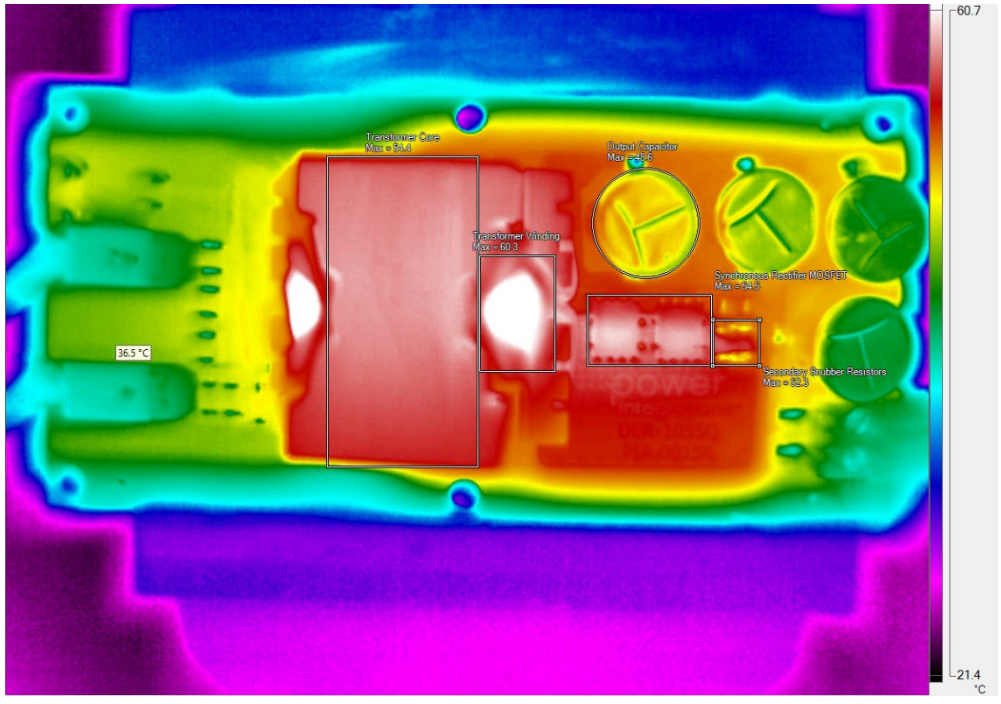


Figure 32 – PCB Top Thermal Scan at 190 V Input.

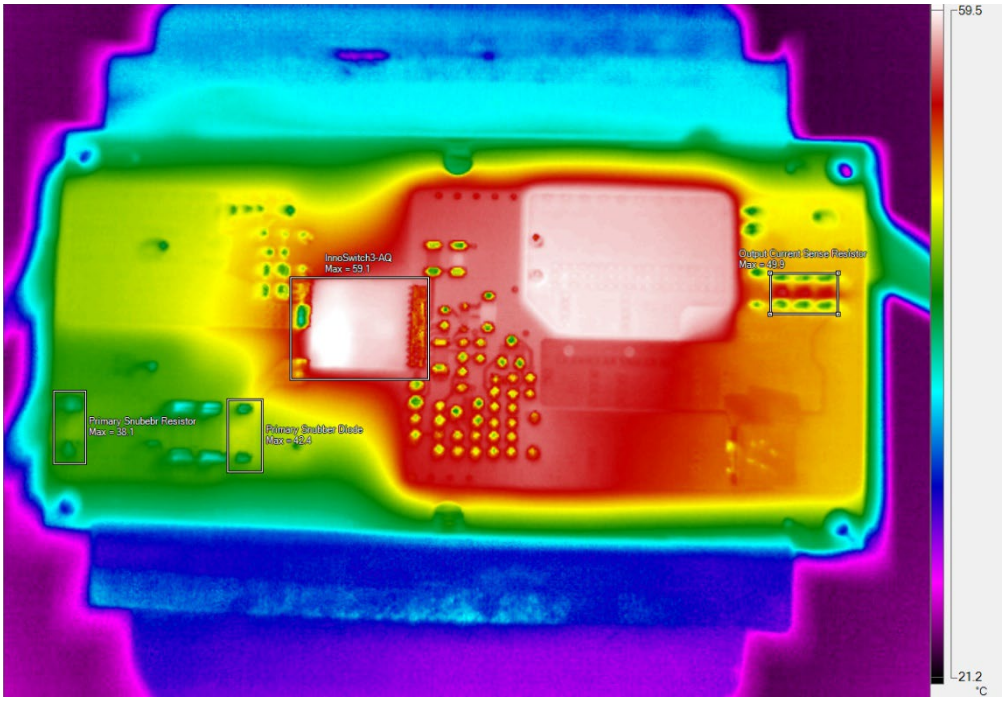


Figure 33 – PCB Bottom Thermal Scan at 450 V Input.

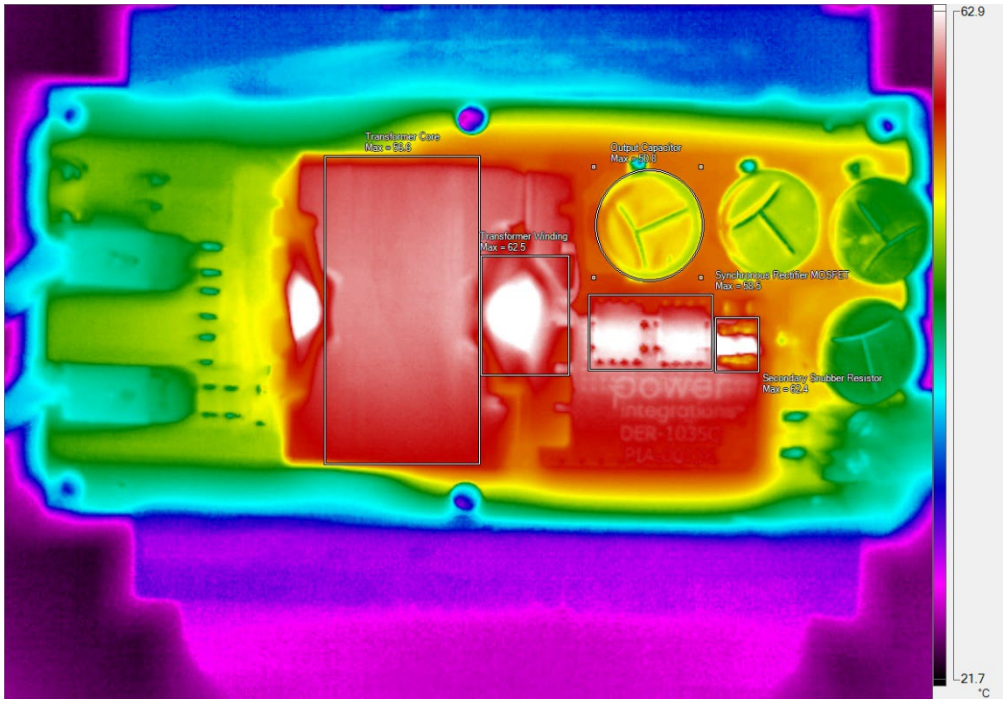


Figure 34 – PCB Top Thermal Scans at 450 V Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit under test to a fully charged DC link capacitor[11] at different test input voltages. An electronic load configured for constant resistance was used for all start-up tests.

11.1.1 Output Voltage and Current at 85 °C[12,13]

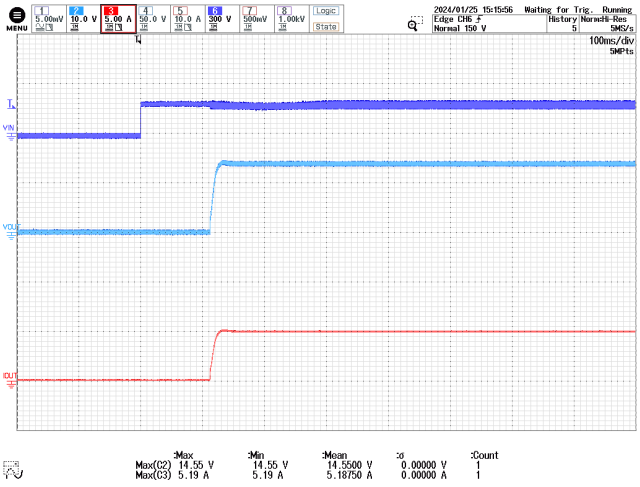


Figure 35 – Output Voltage and Current.
190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

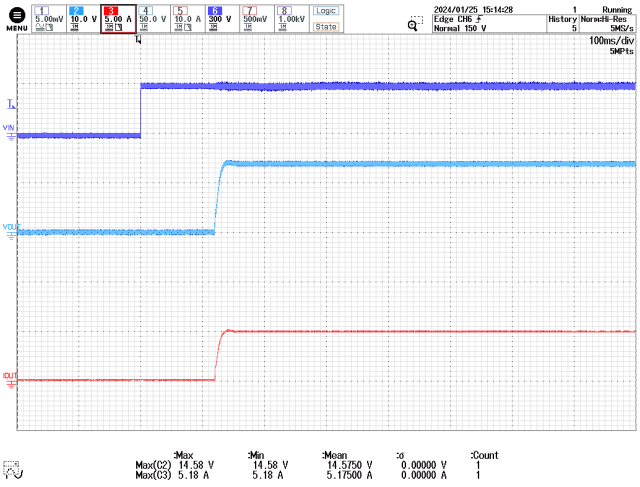


Figure 36 – Output Voltage and Current.
300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

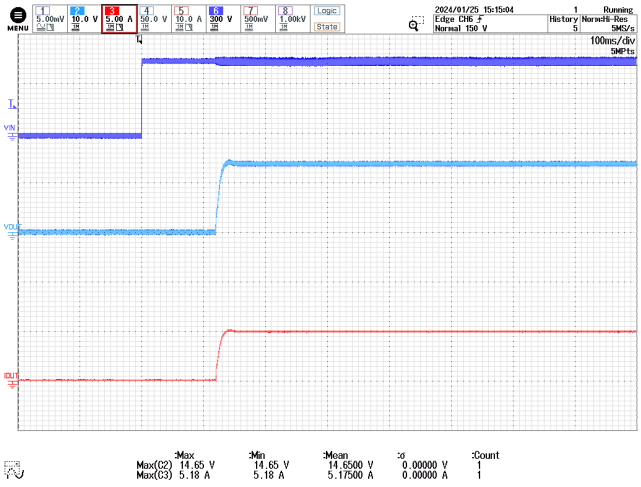


Figure 37 – Output Voltage and Current.
450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

[11] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[12] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[13] Current waveforms were measured using a Yokogawa current probe

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C[14,15]

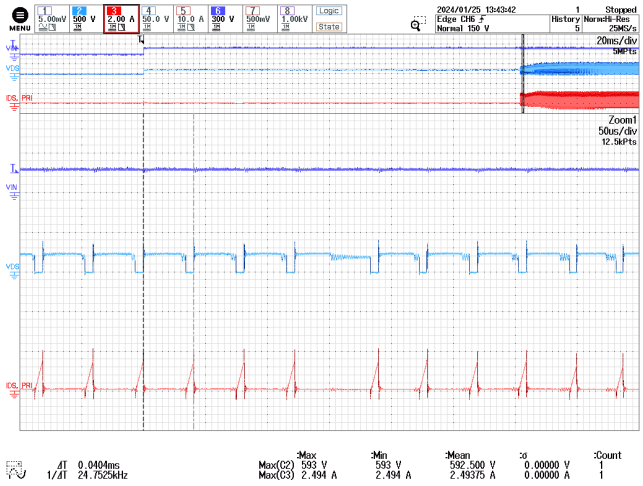


Figure 38 – INN3949CQ Drain Voltage and Current.
190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 20 ms / div.

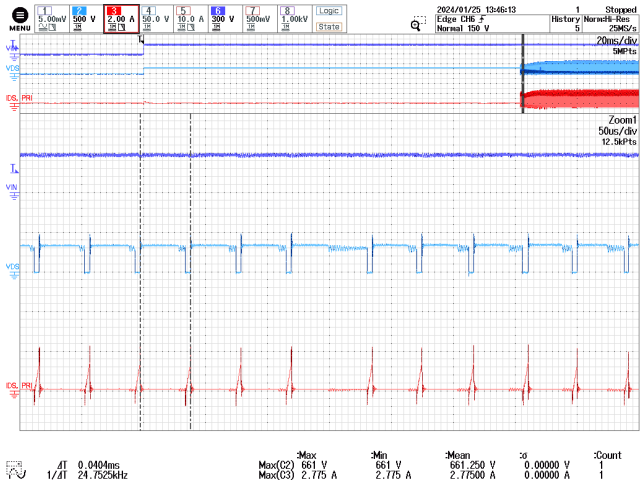


Figure 39 – INN3949CQ Drain Voltage and Current.
300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 20 ms / div.

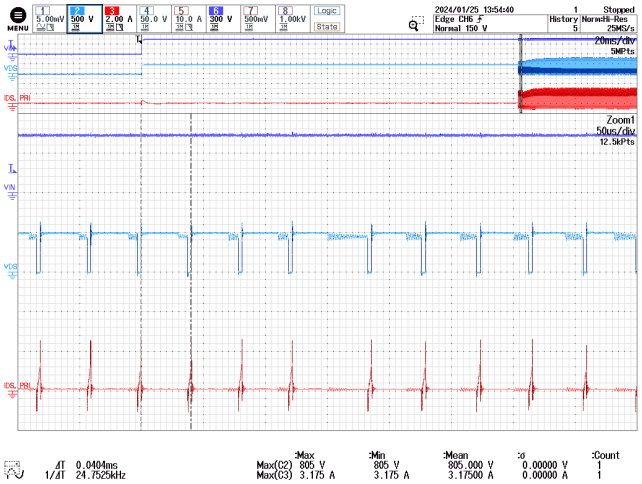


Figure 40 – INN3949CQ Drain Voltage and Current.
450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 20 ms / div.

[14] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[15] Current waveforms were measured using a 30 A rogowski current probe.

11.1.3 SR FET Drain Voltage and Current at 85 °C[16,17]

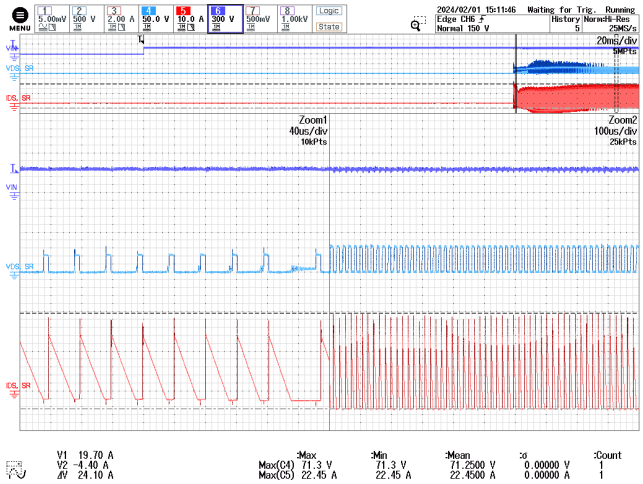


Figure 41 – SR FET Drain Voltage and Current.
190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH4: V_{OUT}, 50 V / div.
CH5: I_{OUT}, 10 A / div.
Time: 20 ms / div.

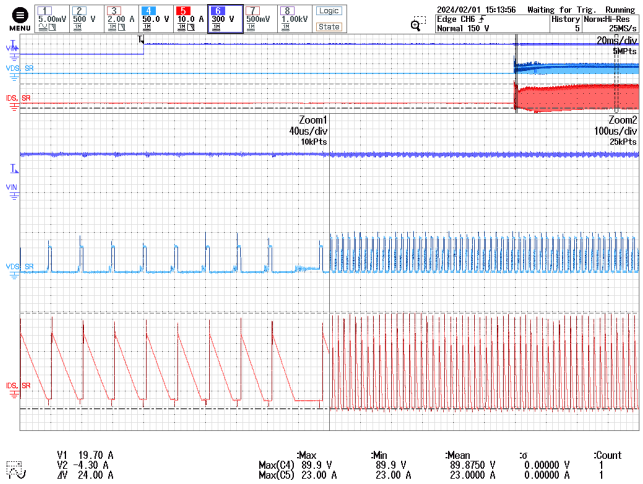


Figure 42 – SR FET Drain Voltage and Current.
Vin = 300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH4: V_{OUT}, 50 V / div.
CH5: I_{OUT}, 10 A / div.
Time: 20 ms / div.

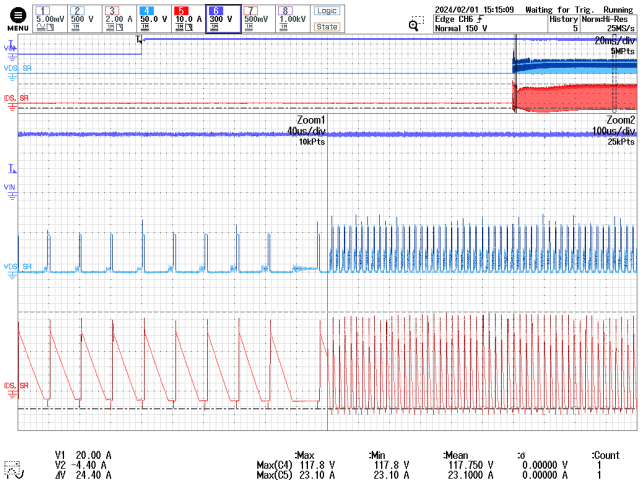


Figure 43 – SR FET Drain Voltage and Current.
Vin = 450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH4: V_{OUT}, 50 V / div.
CH5: I_{OUT}, 10 A / div.
Time: 20 ms / div.

[16] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[17] Current waveforms were measured using a 120 A rogowski current probe.

11.1.4 Output Voltage and Current at -40 °C[18,19]

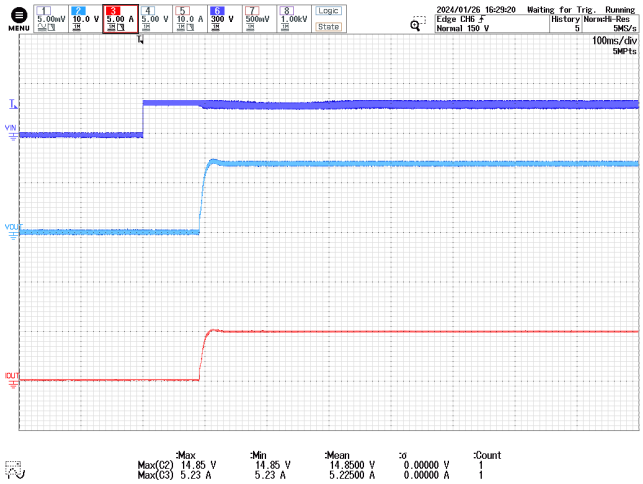


Figure 44 – Output Voltage and Current.
Vin = 190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

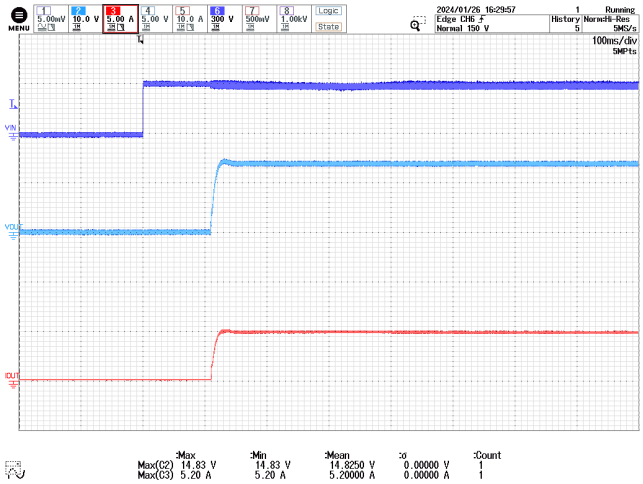


Figure 45 – Output Voltage and Current.
Vin = 300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

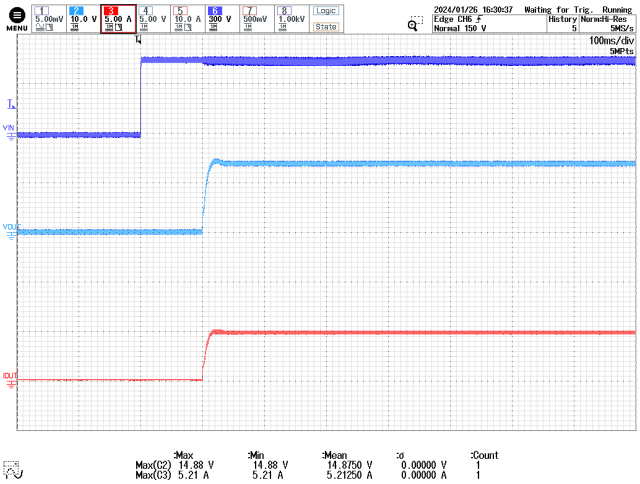


Figure 46 – Output Voltage and Current.
Vin = 450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 100 ms / div.

[18] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[19] Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C[20,21]

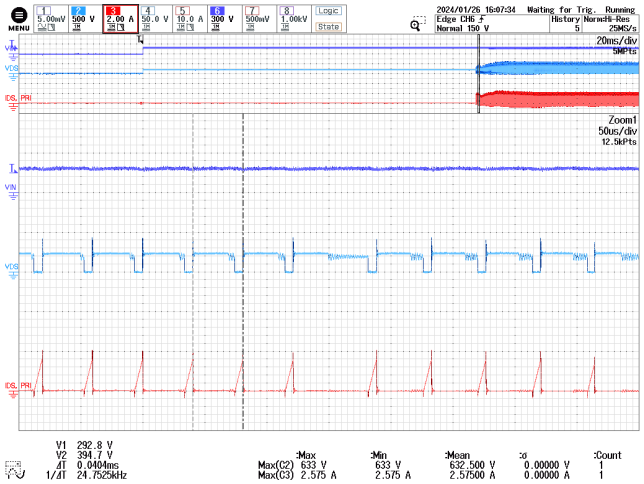


Figure 47 – INN3949CQ Drain Voltage and Current.
Vin = 190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.

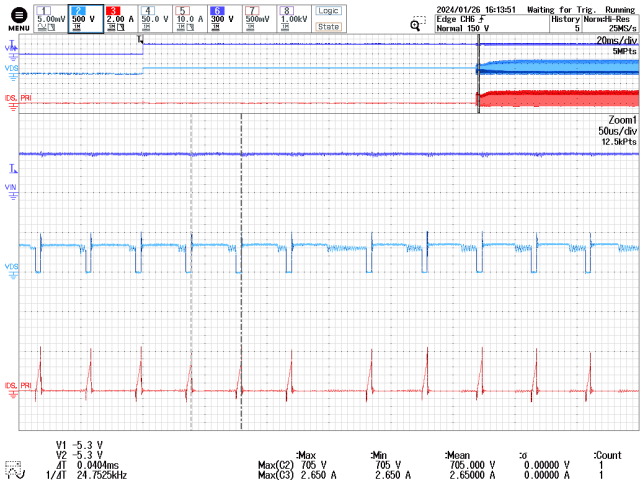


Figure 48 – INN3949CQ Drain Voltage and Current.
Vin = 300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.

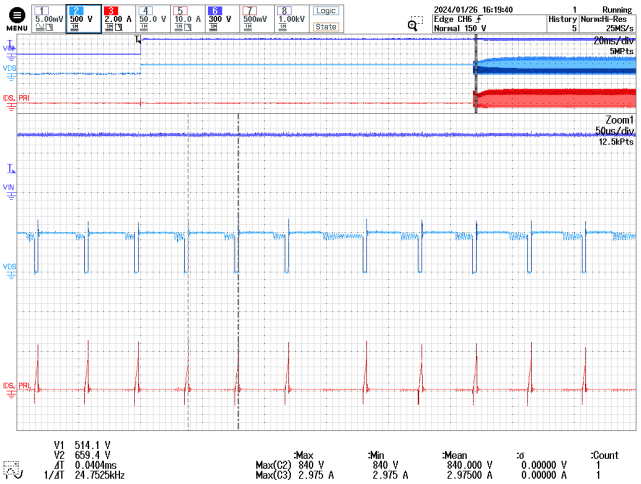


Figure 49 – INN3949CQ Drain Voltage and Current.
Vin = 450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 500 V / div.
CH3: I_{OUT}, 2 A / div.
Time: 100 ms / div.

[20] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[21] Current waveforms were measured using a 30 A Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at -40 °C[22,23]

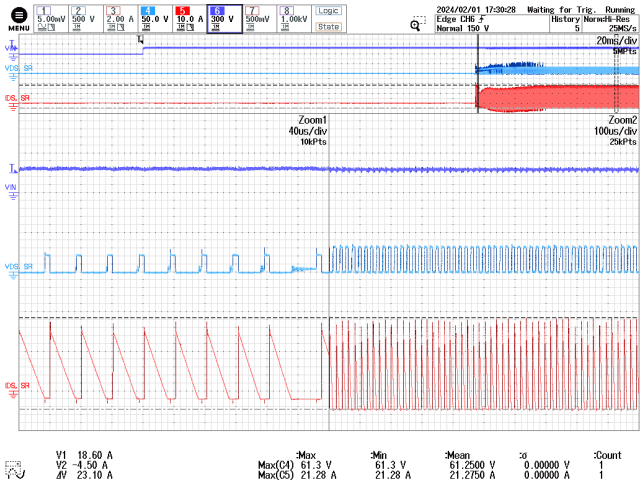


Figure 50 – SR FET Drain Voltage and Current.
Vin = 190 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 50 V / div.
CH3: I_{OUT}, 10 A / div.
Time: 100 ms / div.

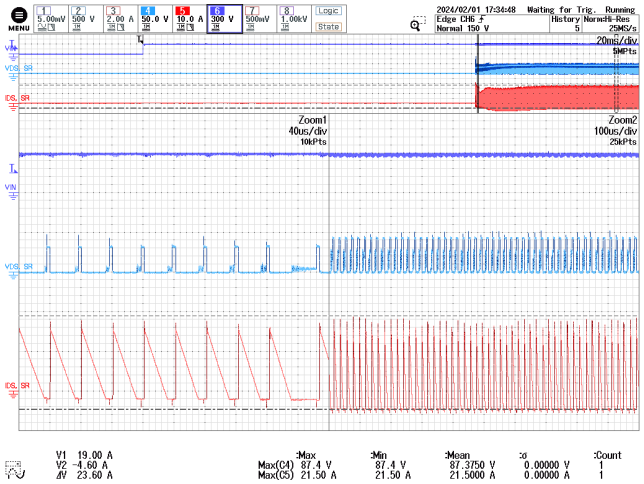


Figure 51 – SR FET Drain Voltage and Current.
Vin = 300 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 50 V / div.
CH3: I_{OUT}, 10 A / div.
Time: 100 ms / div.

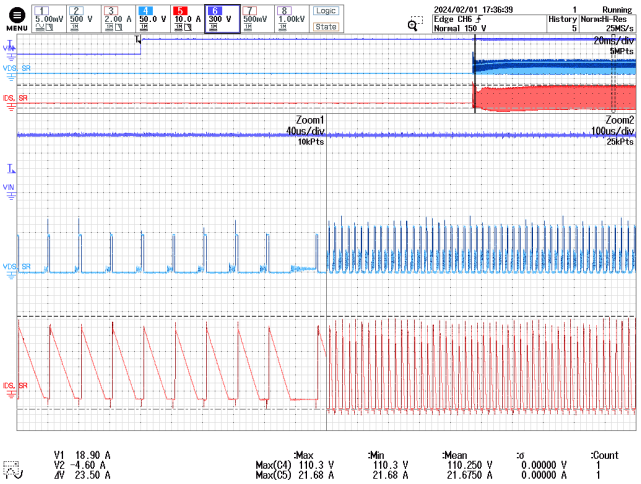


Figure 52 – SR FET Drain Voltage and Current.
Vin = 450 V_{DC}, 2.8 Ω Load.
CH6: V_{IN}, 300 V / div.
CH2: V_{OUT}, 50 V / div.
CH3: I_{OUT}, 10 A / div.
Time: 100 ms / div.

[22] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additiona t_{AR} delay of InnoSwitch3.
[23] Current waveforms were measured using a 120 A Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C

11.2.1.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR FETs**		
V_{IN}(V)	**$I_D(A_{PK})$**	**$V_{DS}(V_{PK})$**	**V_{STRESS} (%)**	**$I_D(A_{PK})$[24]**	**$V_{DS}(V_{PK})$[25]**	**V_{STRESS} (%)**
190	1.6	553	52.5	23.5	54.4	36.3
300	1.525	668	39.3	24.1	54.9	36.6
450	1.425	819	48.2	24.3	75.1	50

Table 11 – Summary of Critical Component Voltage Stresses at 85 °C Ambient Temperature.

[24] SR FET current is the sum of Q100 and Q101 currents.
[25] SR FET voltage was taken from Q101.

11.2.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C[26]

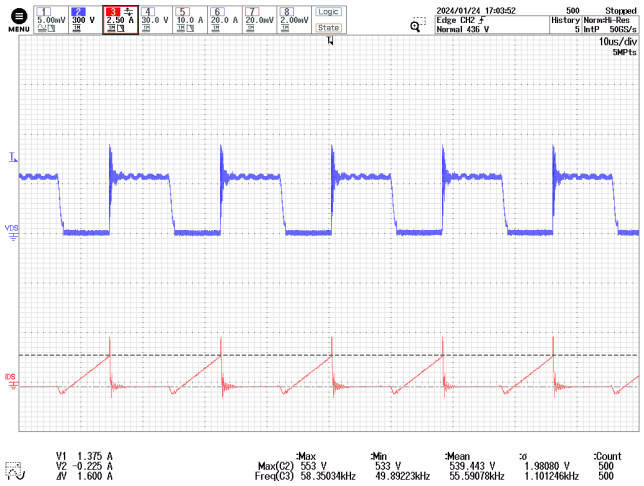


Figure 53 – INN3949CQ Drain Voltage and Current.
Vin = 190 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

Figure 54 – INN3949CQ Drain Voltage and Current.
V in = 300 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

Figure 55 – INN3949CQ Drain Voltage and Current.
Vin = 450 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

[26] Current is measured using a 30 A Rogowski probe

11.2.1.3 SR-FET Drain Voltage and Current at 85 °C[27]

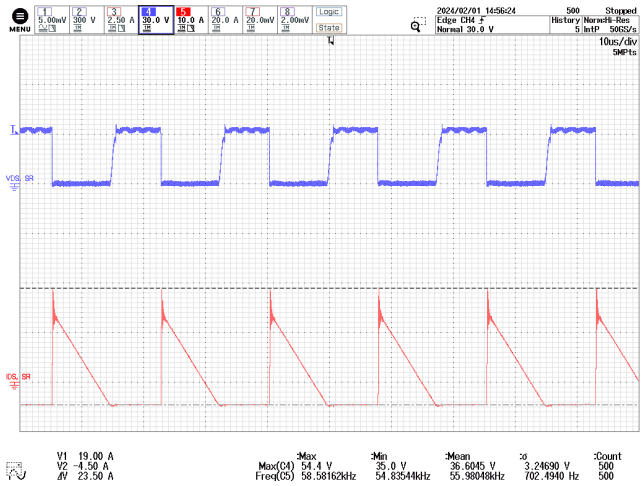


Figure 56 – SR FET Drain Voltage and Current.
Vin = 190 V_{DC}, 5 A Load.
CH4: $V_{DS,INNO}$, 50 V / div.
CH5: $I_{DS,INNO}$, 10 A / div.
Time: 10 μs / div.

Figure 57 – SR FET Drain Voltage and Current.
Vin = 300 V_{DC}, 5 A Load.
CH4: $V_{DS,INNO}$, 50 V / div.
CH5: $I_{DS,INNO}$, 10 A / div.
Time: 10 μs / div.

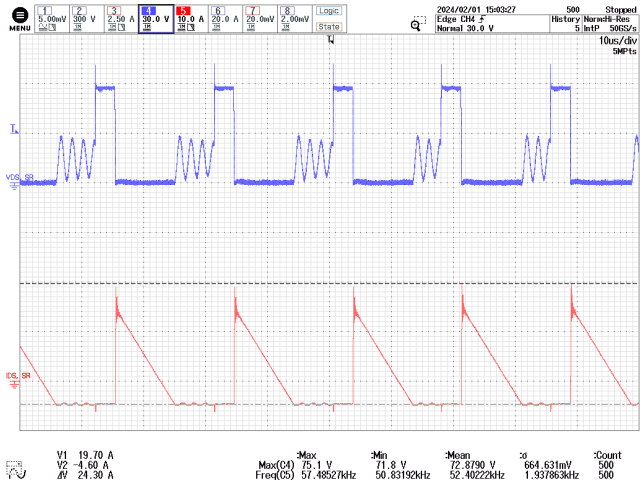


Figure 58 – SR FET Drain Voltage and Current.
Vin = 450 V_{DC}, 5 A Load.
CH4: $V_{DS,INNO}$, 50 V / div.
CH5: $I_{DS,INNO}$, 10 A / div.
Time: 10 μs / div.

[27] Current is measured using a 120 A Rogowski probe

11.2.2 Switching Waveforms at -40 °C

11.2.2.1 Normal Operation Component Stress

	Steady-State Switching Waveforms -40 °C Ambient, Full Load					
Input	**INN3990CQ**			**SR FETs**		
V_{IN} (V)	**$I_D(A_{PK})$**	**$V_{DS}(V_{PK})$**	**V_{STRESS} (%)**	**$I_D(A_{PK})$[28]**	**$V_{DS}(V_{PK})$[29]**	**V_{STRESS} (%)**
190	2.575	599	35.2	23.5	37.6	25
300	2.75	718	42.2	23.3	54.4	36.3
450	2.925	843	59.6	23.3	74	49.3

Table 12 – Summary of Critical Component Voltage Stresses at -40 °C Ambient Temperature.

[28] SR FET current is the sum of Q100 and Q101 currents.
[29] SR FET voltage was taken from Q101.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at -40 °C[30]

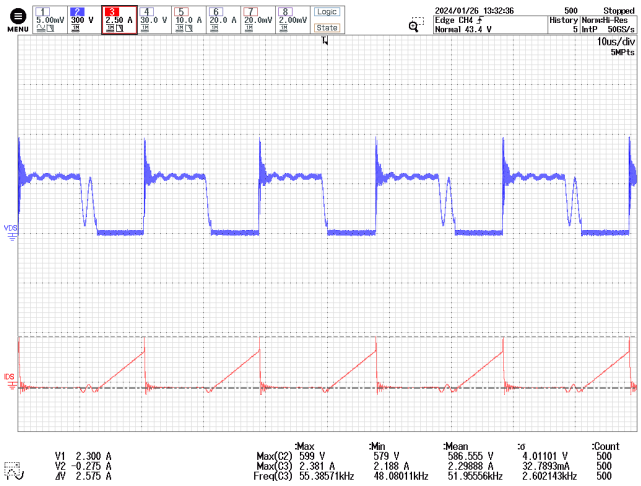


Figure 59 – INN3949CQ Drain Voltage and Current.
Vin = 190 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

Figure 60 – INN3949CQ Drain Voltage and Current.
Vin = 300 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

Figure 61 – INN3949CQ Drain Voltage and Current.
Vin = 450 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 300 V / div.
CH3: $I_{DS,INNO}$, 2.5 A / div.
Time: 10 μs / div.

[30] Current is measured using a 30 A Rogowski probe

11.2.2.3 SR FET Drain Voltage and Current at -40 °C[31]

Figure 62 – SR FET Drain Voltage and Current.
Vin = 190 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 µs / div.

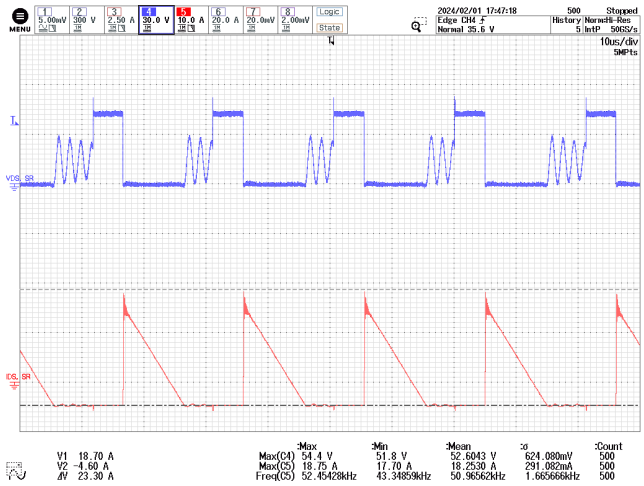


Figure 63 – SR FET Drain Voltage and Current.
Vin = 300 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 µs / div.

Figure 64 – SR FET Drain Voltage and Current.
Vin = 450 V_{DC}, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 µs / div.

[31] Current is measured using a 120 A Rogowski probe

11.2.2.4 Short-Circuit Response at 85 °C

The unit was tested by applying an output short-circuit during normal working conditions and then removing the short-circuit to see if the unit could recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto-restart) mode and attempt recovery every 1.7 to 2.11 seconds. Full load configuration is at 1.835 Ω constant resistance.

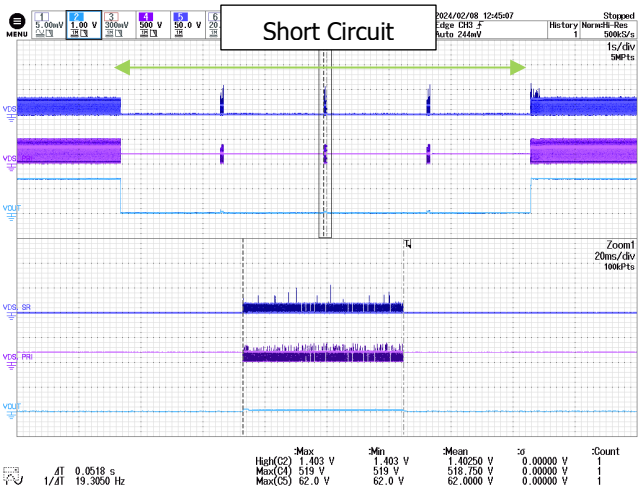


Figure 65 – INN3949CQ and SR FET Drain Voltage.
Vin = 190 V_{DC}, 2.8 Ω-Short-2.8 Ω.
CH2: V_{OUT}, 10 V / div.
CH4: $V_{DS,PRI}$, 500 V / div.
CH5: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

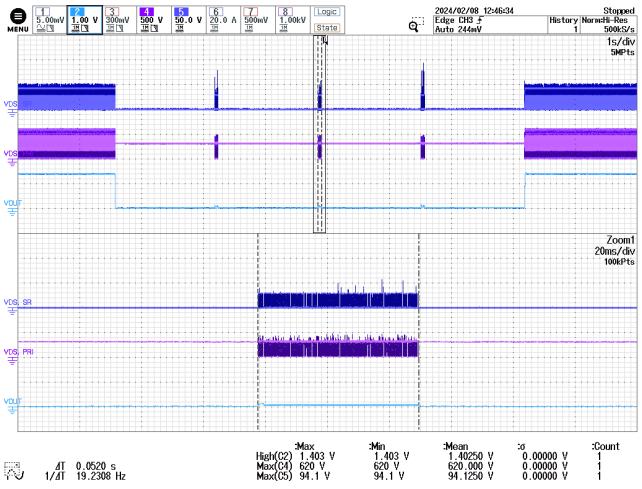


Figure 66 – INN349CQ and SR FET Drain Voltage.
Vin = 300 V_{DC}, 2.8 Ω-Short-2.8 Ω.
CH2: V_{OUT}, 10 V / div.
CH4: $V_{DS,PRI}$, 500 V / div.
CH5: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

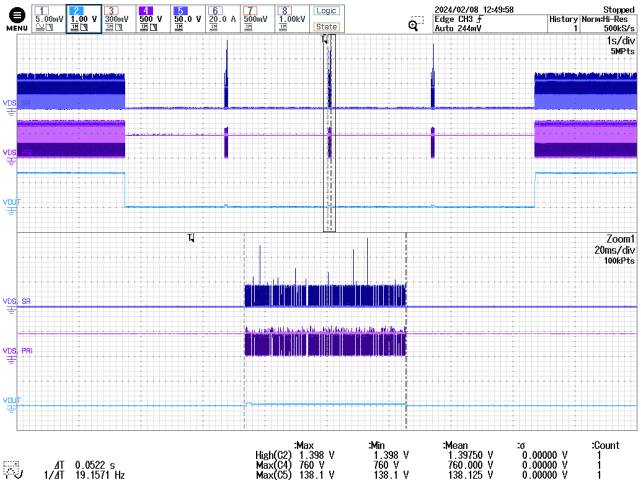


Figure 67 – INN3949CQ and SR FET Drain Voltage.
Vin = 450 V_{DC}, 2.8 Ω-Short-2.8 Ω.
CH2: V_{OUT}, 10 V / div.
CH4: $V_{DS,PRI}$, 500 V / div.
CH5: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

11.3 Load Transient Response

Output voltage waveform on the board was captured with dynamic load transient from 10% to 90%. The duration for the load states is set to 500 ms, and the load slew rate is 400 mA / μs. The test is done at 85 °C ambient temperature with 10 samples taken per case.

Dynamic Load Settings	V_{IN} (V)	ΔV_+ (V)	ΔV_- (V)
10% to 90%	190	0.113	-0.173
	300	0.102	-0.162
	450	0.098	-0.174

Table 13 – Load Transient Response.

11.3.1 Output Voltage Ripple with 10% to 90% Transient Load at 85 °C

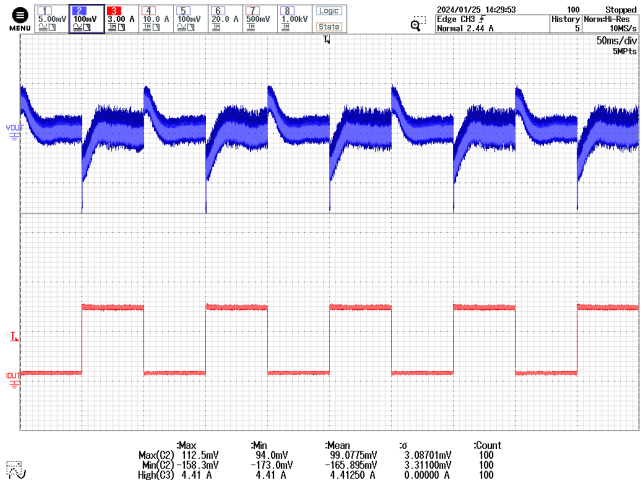


Figure 68 – Output Voltage and Current.
190 V_{DC}, 0.5 A to 4.95 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE}, 100 mV / div.
CH3: I_{OUT}, 3 A / div.
Time: 50 ms / div.

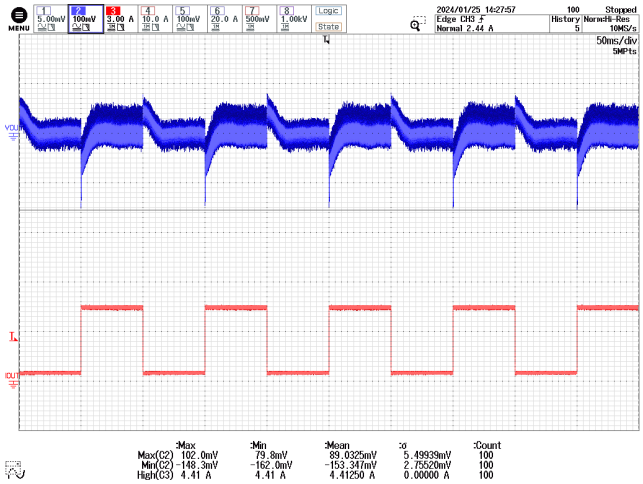


Figure 69 – Output Voltage and Current.
300 V_{DC}, 0.5 A to 4.95 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE}, 100 mV / div.
CH3: I_{OUT}, 3 A / div.
Time: 50 ms / div.

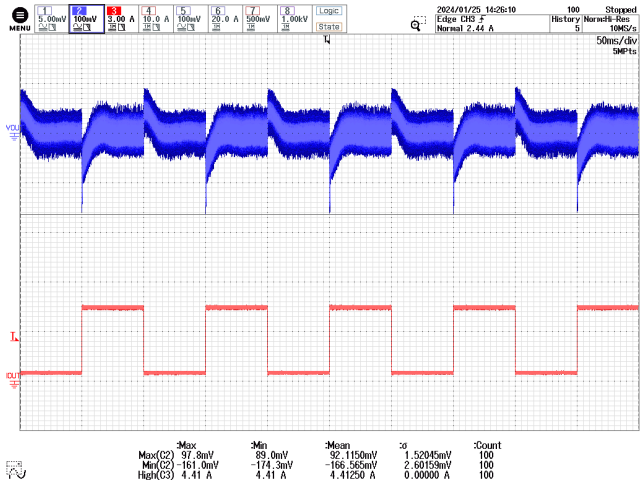


Figure 70 – Output Voltage and Current.
450 V_{DC}, 0.5 A to 4.95 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE}, 100 mV / div.
CH3: I_{OUT}, 3 A / div.
Time: 50 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe must be utilized for DC output ripple measurements to reduce spurious signals due to noise pick-up. Details of the probe modification are provided in Figure 71 and Figure 72 below.

A CT2708 probe adapter is affixed with a 10 μF / 50 V electrolytic capacitor in parallel with a 1 μF / 50 V ceramic capacitor across the probe tip. Coaxial wires kept as short as possible are soldered directly to the probe and the output terminals.

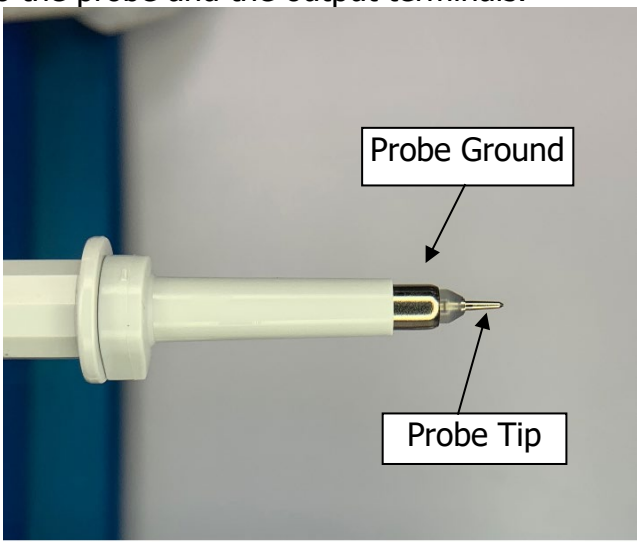


Figure 71 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

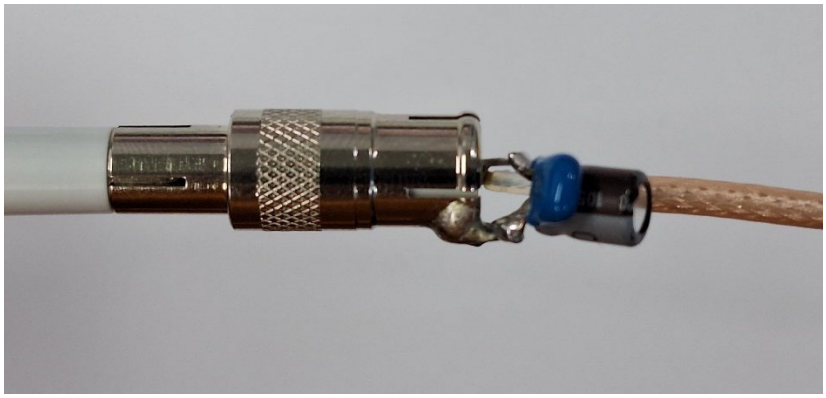


Figure 72 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurements, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform was captured at the output terminals using the ripple measurement probe with a decoupling capacitor. The waveforms shown are taken at the load setting where the highest ripple was observed for every input voltage setting.

11.4.2.1 Output Voltage Ripple at 85 °C Constant Full Load[32]

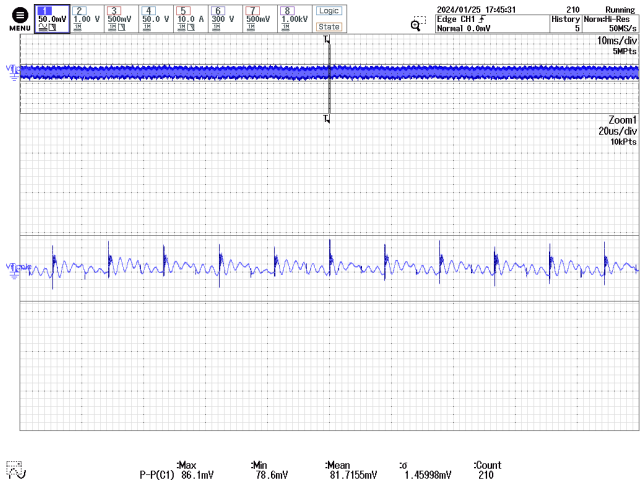


Figure 73 – Output Voltage Ripple.
190 V_{DC}, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 86.1 mV.

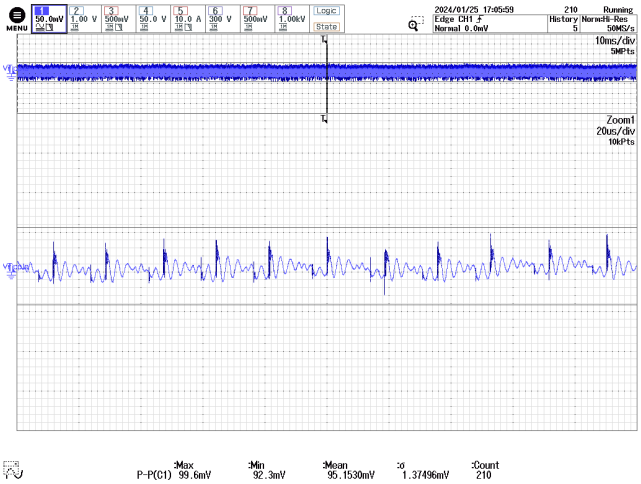


Figure 74 – Output Voltage Ripple.
300 V_{DC}, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 99.6 mV.

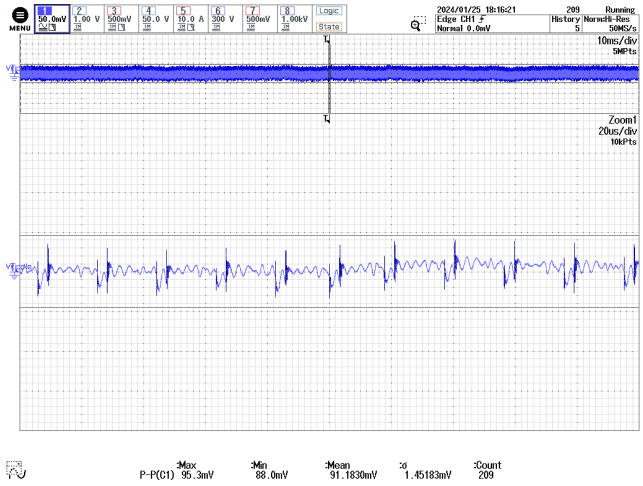


Figure 75 – Output Voltage Ripple.
450 V_{DC}, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 95.3 mV.

[32] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at -40 °C Constant Full Load[33]

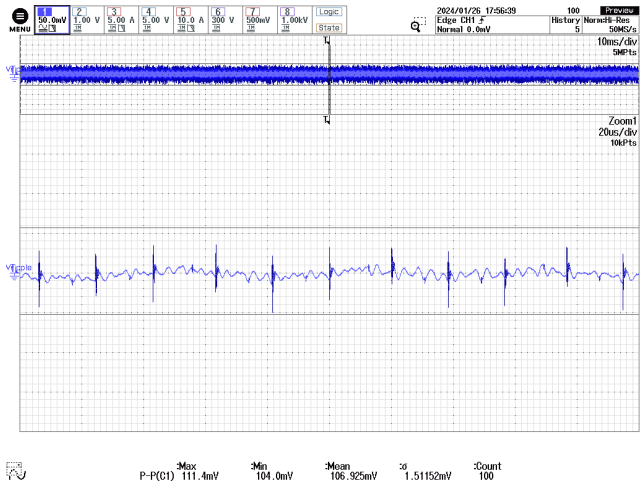


Figure 76 – Output Voltage Ripple.
150 V_{DC}, 4.41 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 150 mV.

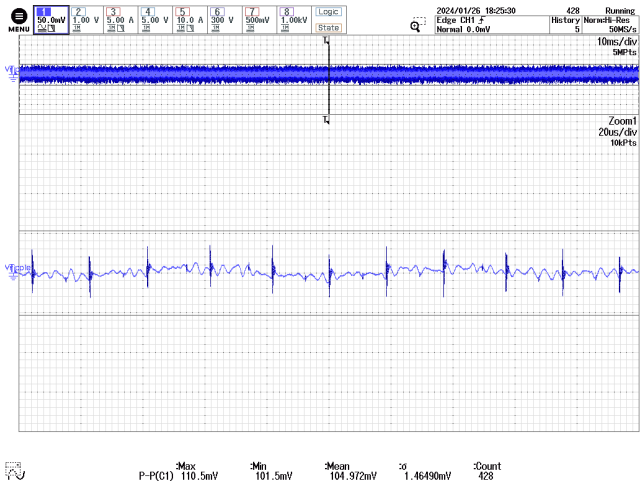


Figure 77 – Output Voltage Ripple.
190 V_{DC}, 6.61 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 141 mV.

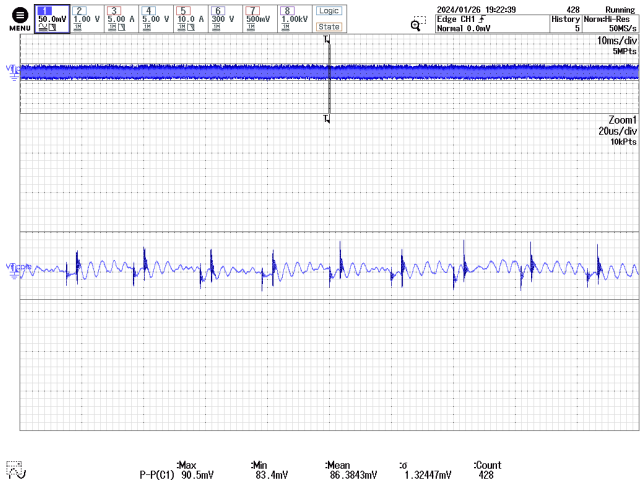


Figure 78 – Output Voltage Ripple.
380 V_{DC}, 5.88 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 103 mV.

[33] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at 25 °C Constant Full Load[34]

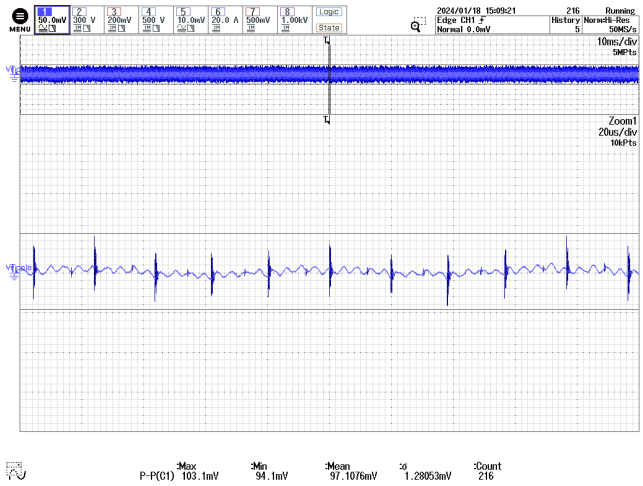


Figure 79 – Output Voltage Ripple.
190 V_{DC}, 5 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 103.1 mV

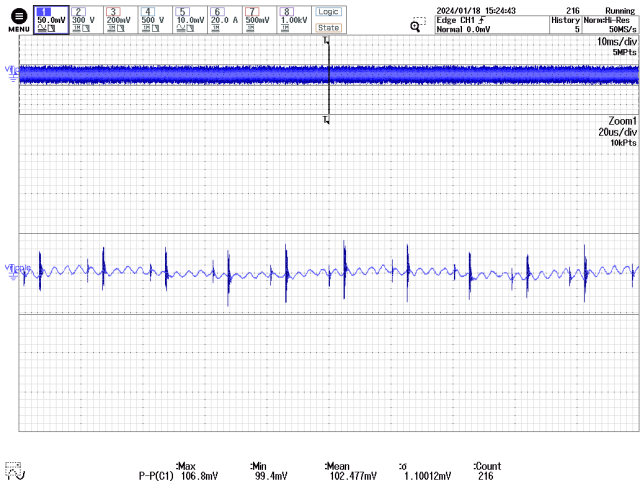


Figure 80 – Output Voltage Ripple.
300 V_{DC}, 5 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 106.8 mV.

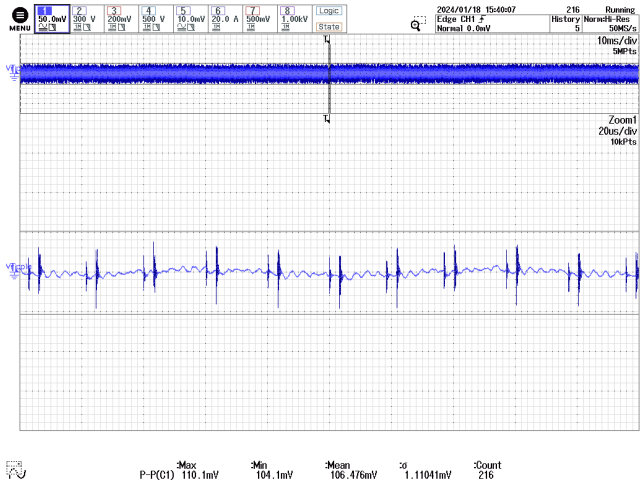


Figure 81 – Output Voltage Ripple.
450 V_{DC}, 5 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 110.1 mV.

[34] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C

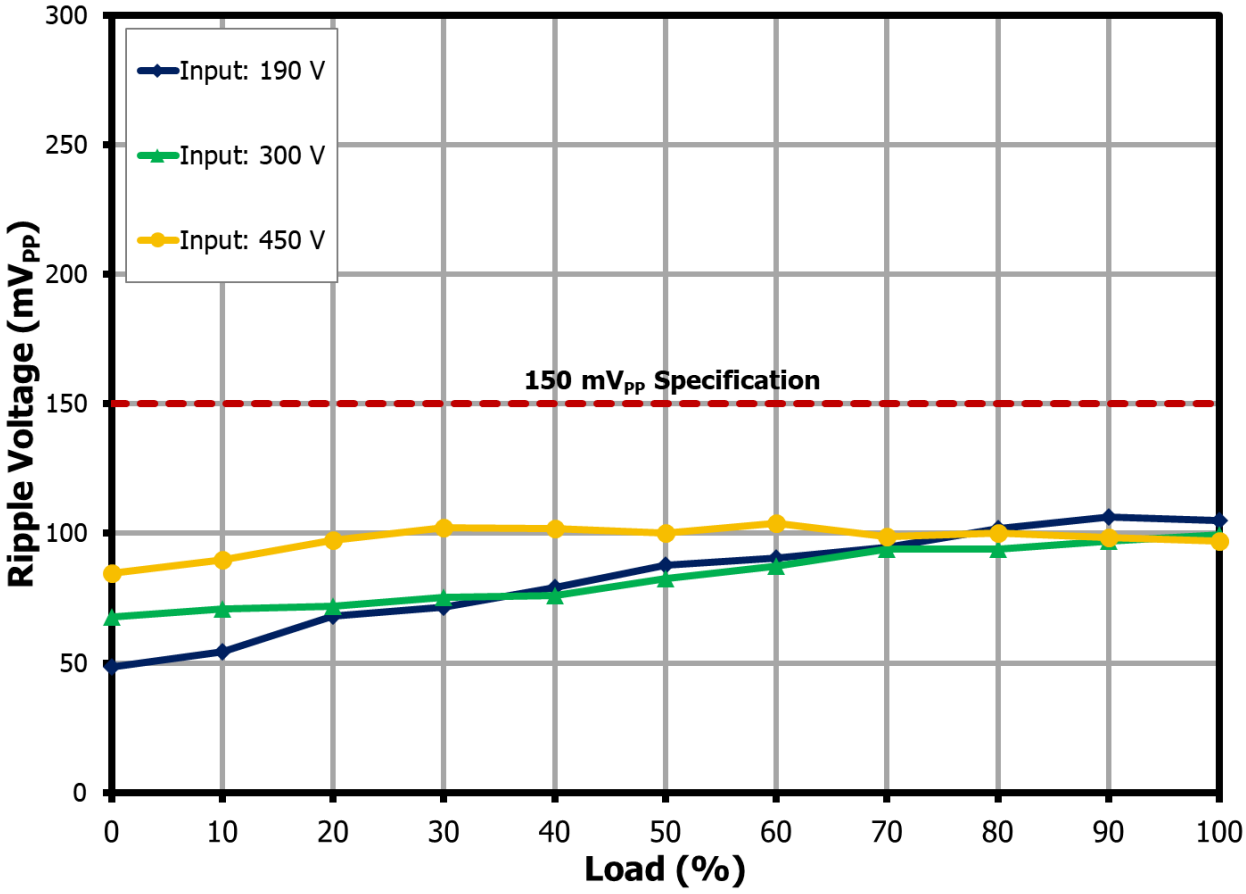


Figure 82 – Output Ripple Voltage Across Whole Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C

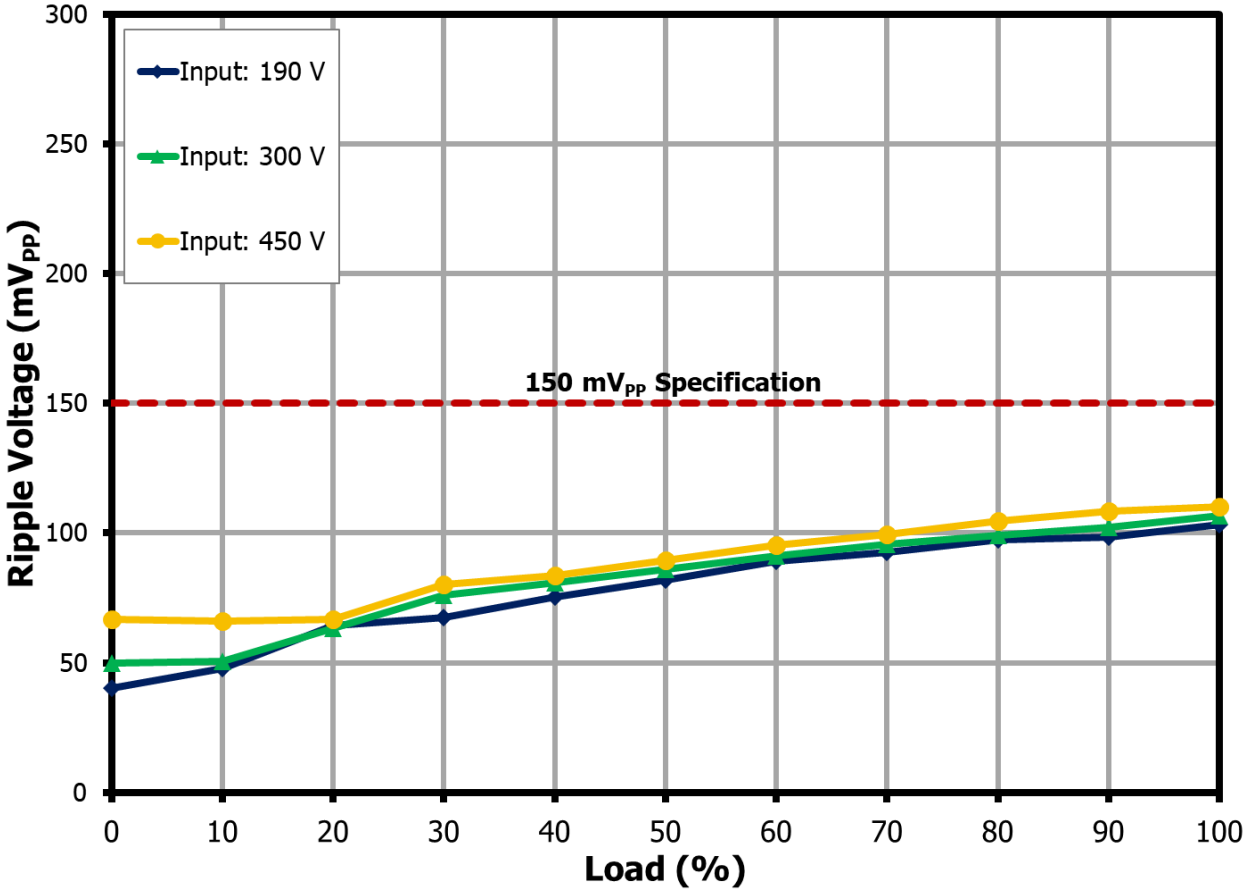


Figure 83 – Output Ripple Voltage Across Whole Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C

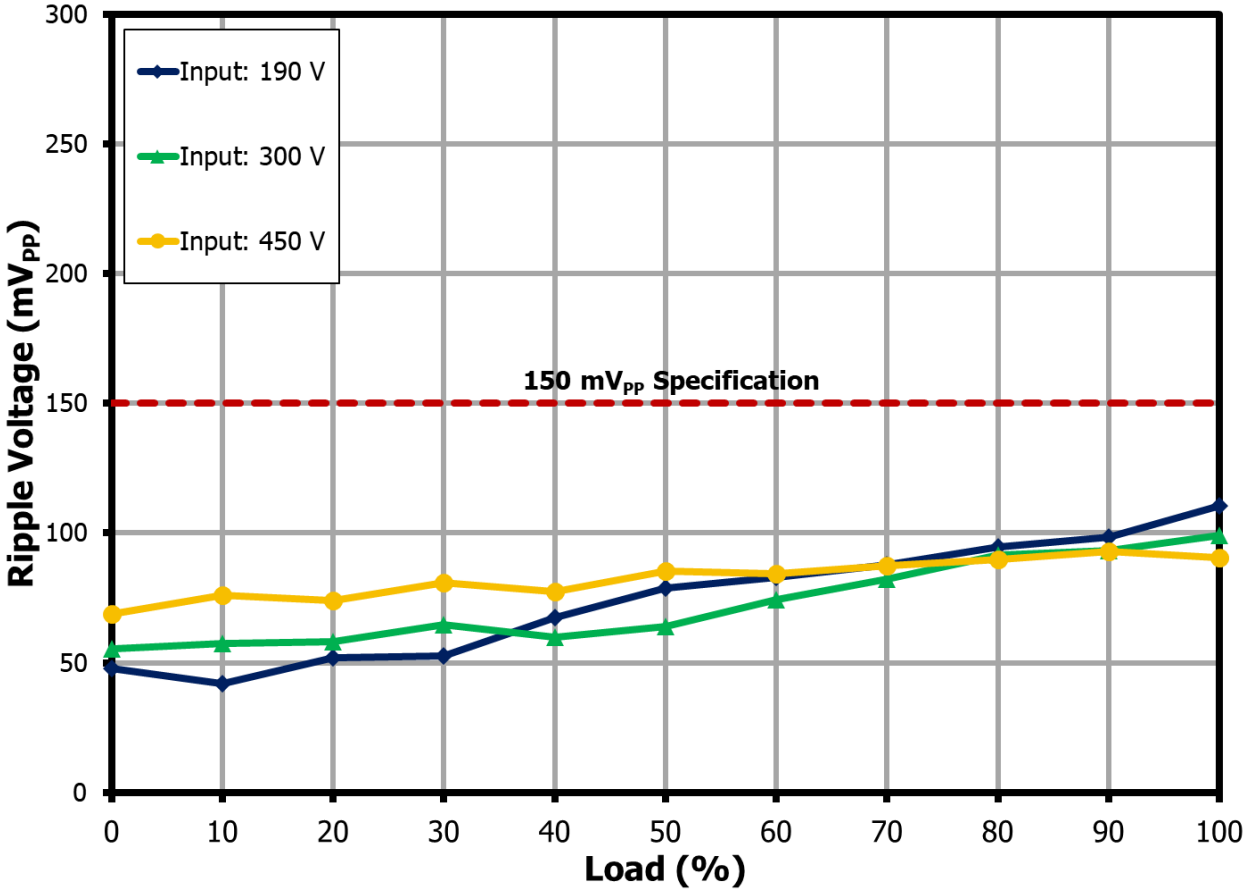


Figure 84 – Output Ripple Voltage Across Whole Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to desired ambient temperature for at least 30 minutes before turning on the unit under test. For every loading condition, unit under test was soaked for at least 60 seconds before the voltage and current measurements on the 14 V output were taken.

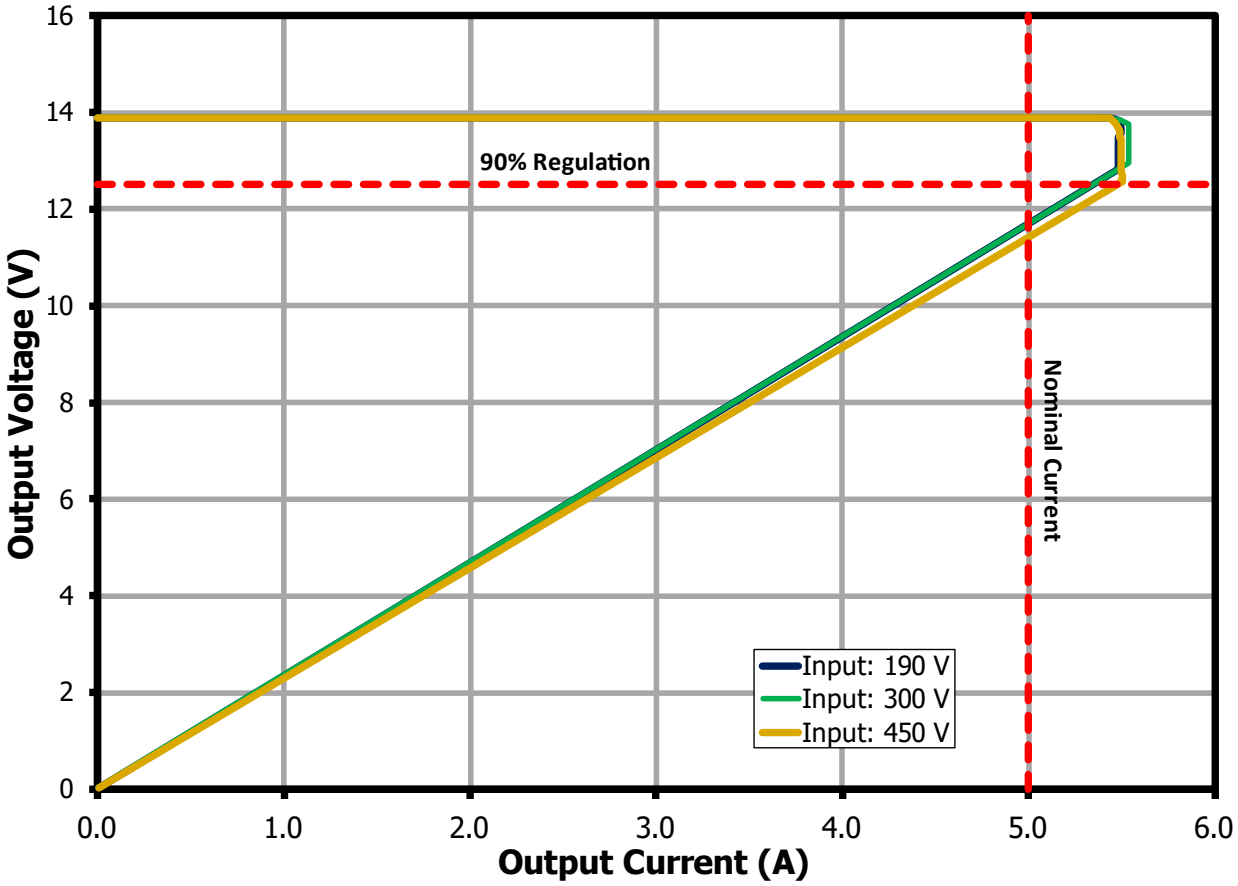


Figure 85 – 14 V Output Overload Curve at 85 °C Ambient Temperature.

13 Maximum Output Power

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C for at least 30 minutes before turning on the unit under test. The unit was soaked for at least 30 minutes for every change in the input voltage and loading condition during the start of each test sequence to allow component temperatures to settle.

Maximum output power capability at a given input voltage was determined by finding the maximum loading condition in which the unit doesn't enter auto-restart (AR) mode operation or trigger any overtemperature protection. Component case temperature ratings for the critical components were also considered in determining the maximum output power capability.

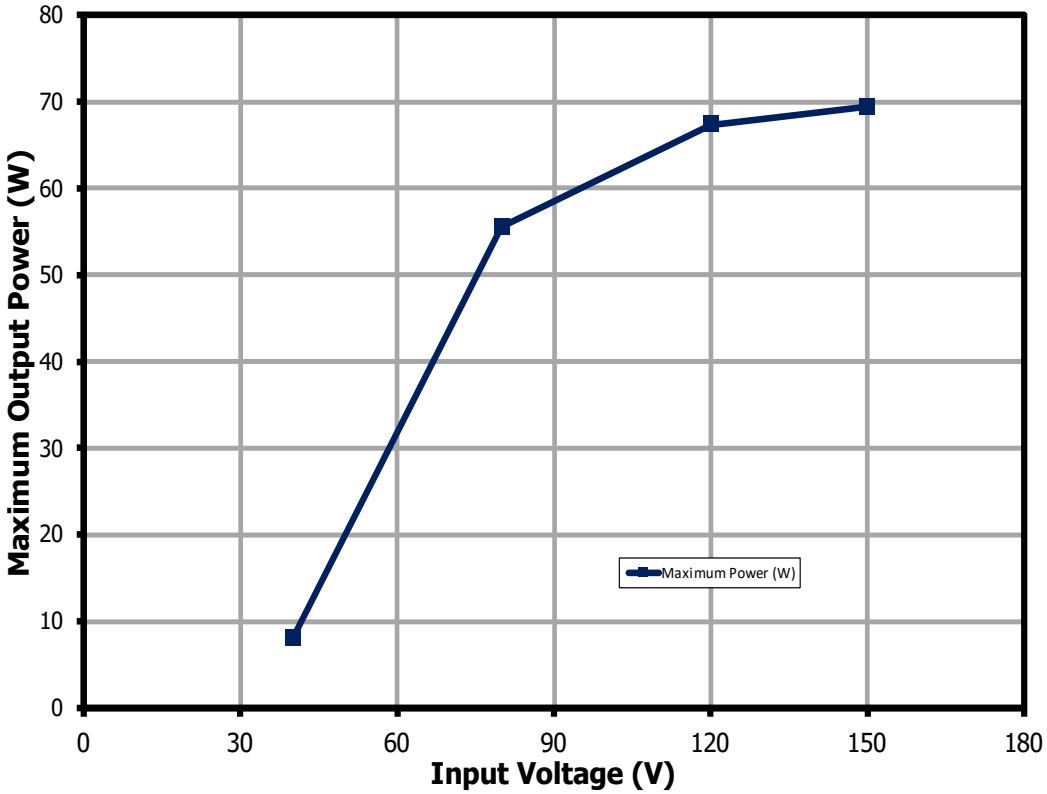


Figure 86 – Maximum Output Power Curve at 85 °C Ambient Temperature.

Input Voltage (V)	Maximum Power (W)	Limiting Factor	Value (ºC)
150	69.42	SR Snubber Temperature	125.15
120	67.31	SR Snubber Temperature	125.15
80	55.54	InnoSwitch3-AQ OverTemperature Protection	128.15
40	8.07	InnoSwitch3-AQ Minimum Off-time	

Table 14 – Maximum Output Power Capability Limiting Factor.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Feb-24	RS	1.0	Initial Release.	CC/JRLC

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