Design Example Report

Title	*13 W Dual Output Automotive Power Supply for 800V Systems Using InnoSwitch™3-AQ INN3949CQ*
Specification	30 V_{DC} – 1000 V_{DC} Input; 18 V / 555 mA; 9 V / 333 mA Outputs
Application	Traction Inverter Gate and/or Emergency Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-956Q
Date	July 31, 2023
Revision	2.0

Summary and Features

- Ultra-compact design for 800 V BEV automotive applications
- Low component count (only 62 components[1]) design with single 1700 V power switch
- Wide range input from 30 V_{DC} to 1000 V_{DC}, start-up and operation
- Reinforced 1000 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥80 % efficiency (450 V_{DC} to 1000 V_{DC})
- Secondary-side regulated output
- Ambient operating temperature -40 °C to 105 °C
- Fully fault protected including output current limit and short-circuit protection
- Uses automotive qualified AEC-Q surface mount (SMD) components[2]

[1] Excluding connectors.
[2] AEC-Q200 transformer and input common mode choke qualification belongs to final design.

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Disclaimer:

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No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations, or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

1 Introduction

This engineering report describes a 13 W dual output automotive power supply. It is intended for use in 800 V battery system electric vehicles supporting an ultra-wide input range of 30 V_{DC} to 1000 V_{DC}. This design utilizes the 1700 V rated INN3949CQ IC from the InnoSwitch3-AQ family of IC’s.

In a typical configuration the 9 V output provides an emergency backup power rail for the control power of the main traction inverter (functional safety requirement for loss of 12 V), the 18 V output provides gate power.

The design provides reinforced isolation both from the High Voltage DC (HVDC) input to the 18 V and 9 V outputs by observing required creepage and clearances as indicated in IEC 60664 parts 1 and 4. Basic isolation is provided between the 18 V and 9 V outputs.

Included in this document are the power supply design specifications, schematic diagram, bill of materials (BOM), magnetics documentation, printed circuit board (PCB) layout and performance data.

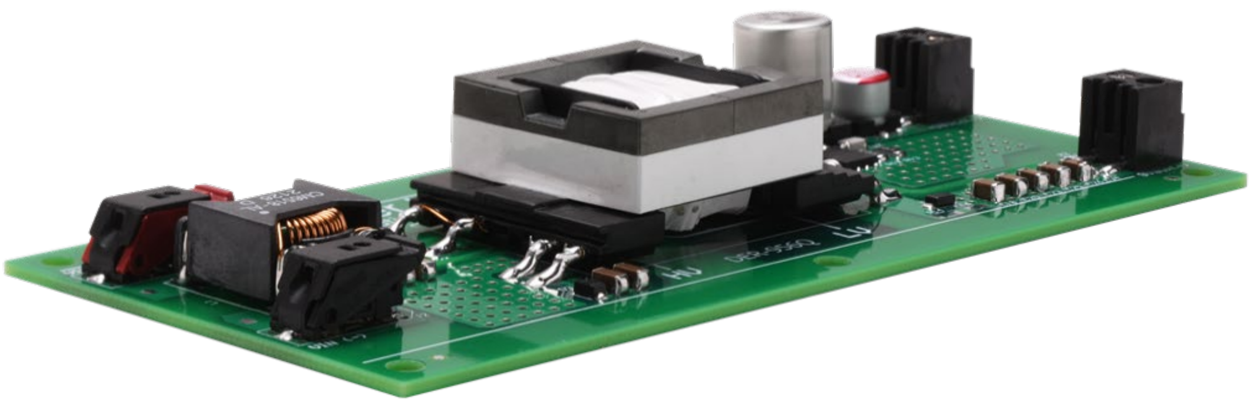

Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

Figure 2 – Populated Circuit Board Photograph, Top.

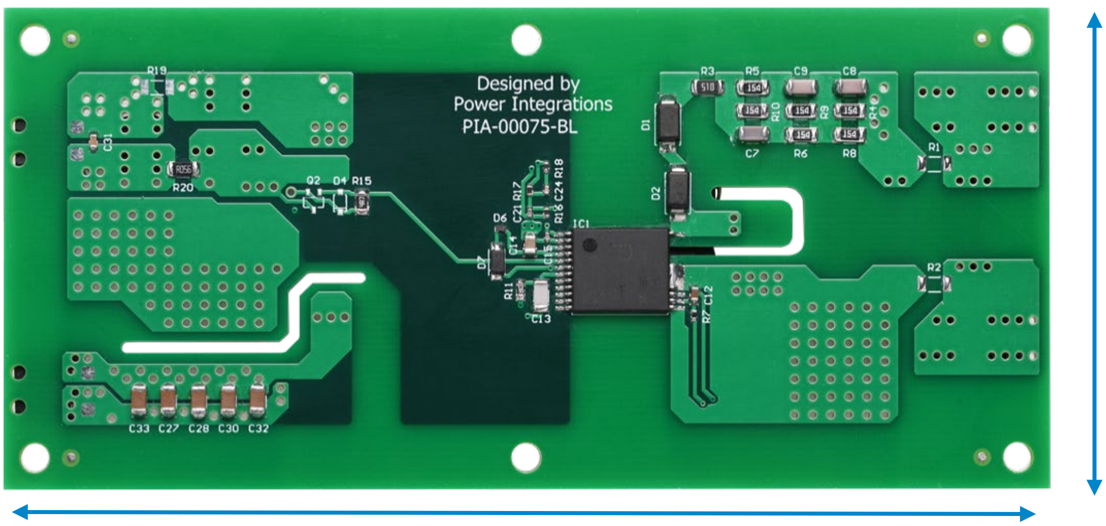

Figure 3 – Populated Circuit Board Photograph, Bottom.

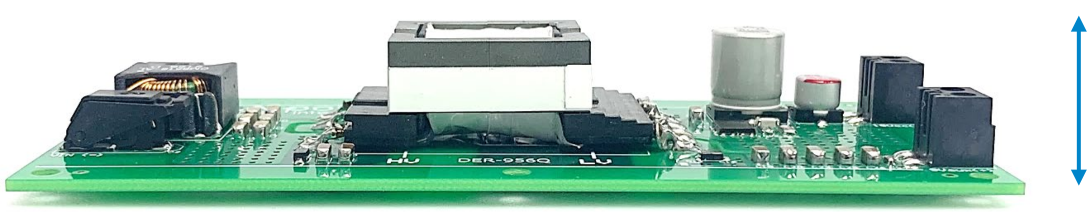

Figure 4 – Populated Circuit Board Photograph, Side.

The regulated 18 V output can deliver 10 W continuously at an input voltage range of 60 V_{DC} to 1000 V_{DC} which can be used to provide gate power for current generation of SiC MOSFETs.

At 30 V_{DC} input, the power capability of 18 V output is reduced to 4 W, enough for startup where the inverter is not being driven. The cross regulated 9 V output can deliver 3 W of power from 30 V_{DC} to 1000 V_{DC} input voltage, providing backup power to maintain inverter operation in the event of the 12 V system failure (functional safety requirement).

The InnoSwitch3-AQ maintains necessary regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink. Secondary-side control also enables the use of synchronous rectification improving the overall efficiency compared to diode rectification thus saving cost and space by eliminating heat sinking.

2 Design Specifications

The table below represents the minimum acceptable performance of the design. The actual performance of the design is listed in the results section.

2.1 *Electrical Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV+**	30	800	1000	V_{DC}
Operating Switching Frequency	f_{SW}	25	33	56	kHz
Output Parameters					
18 V Output					
Output Voltage	$V_{OUT\ (18\ V)}$	17.1	18	18.9	V_{DC}
Load and Line Regulation	$V_{REG\ (18\ V)}$	-5		+5	%
Output Voltage Ripple Measured on Board	$V_{RIPPLE\ (18\ V)}$		500		mV
Output Overshoot / Output Undershoot	$\Delta V_{OUT\ (18\ V)}$		±5		%
Output Current	$I_{OUT\ (18\ V)}$	166	555	610	mA
Continuous Output Power	$P_{OUT(18\ V)}$	3	10		W
9 V Output					
Output Voltage	$V_{OUT\ (9\ V)}$	7.5	9	11	V_{DC}
Load and Line Regulation	$V_{REG\ (9\ V)}$	-17		+22	%
Output Voltage Ripple Measured on Board	$V_{RIPPLE\ (9\ V)}$		800		mV
Output Overshoot / Output Undershoot	$\Delta V_{OUT\ (9\ V)}$	-20		+7	%
Output Current	$I_{OUT\ (9\ V)}$	22		333	mA
Continuous Output Power	$P_{OUT(9\ V)}$	0.2		3	W
Total Output Power Derating					
Continuous Output Power at 30 V_{DC} Input	P_{OUT}			7	W
Continuous Output Power at 60 V_{DC} to 1000 V_{DC} Input				13	W

Table 1 – Electrical Requirements.

2.2 *Isolation Coordination*

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1202	V
Working Voltage	$V_{WORKING}$			1000	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175		399	
Rated Impulse Voltage	$V_{IMPULSE}$			2.5	kV
Altitude Correction Factor for h_a	c_{ha}			1.59	
Technical Cleanliness Requirement				0.6	mm
Basic Clearance Distance Requirement	CLR_{BASIC}	3.0			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	5.4			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	5.6			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	10.6			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	V_{ISO}	5000			V_{PK}
Partial Discharge Test Voltage	V_{PD_TEST}	1803			V_{PK}

Table 2 – Isolation Requirements[3].

2.3 *Environmental Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_a	-40		105	°C
Altitude of Operation	h_a			5500	m
Relative Humidity	**RH**			85	%

Table 3 – Environmental Requirements.

[3] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

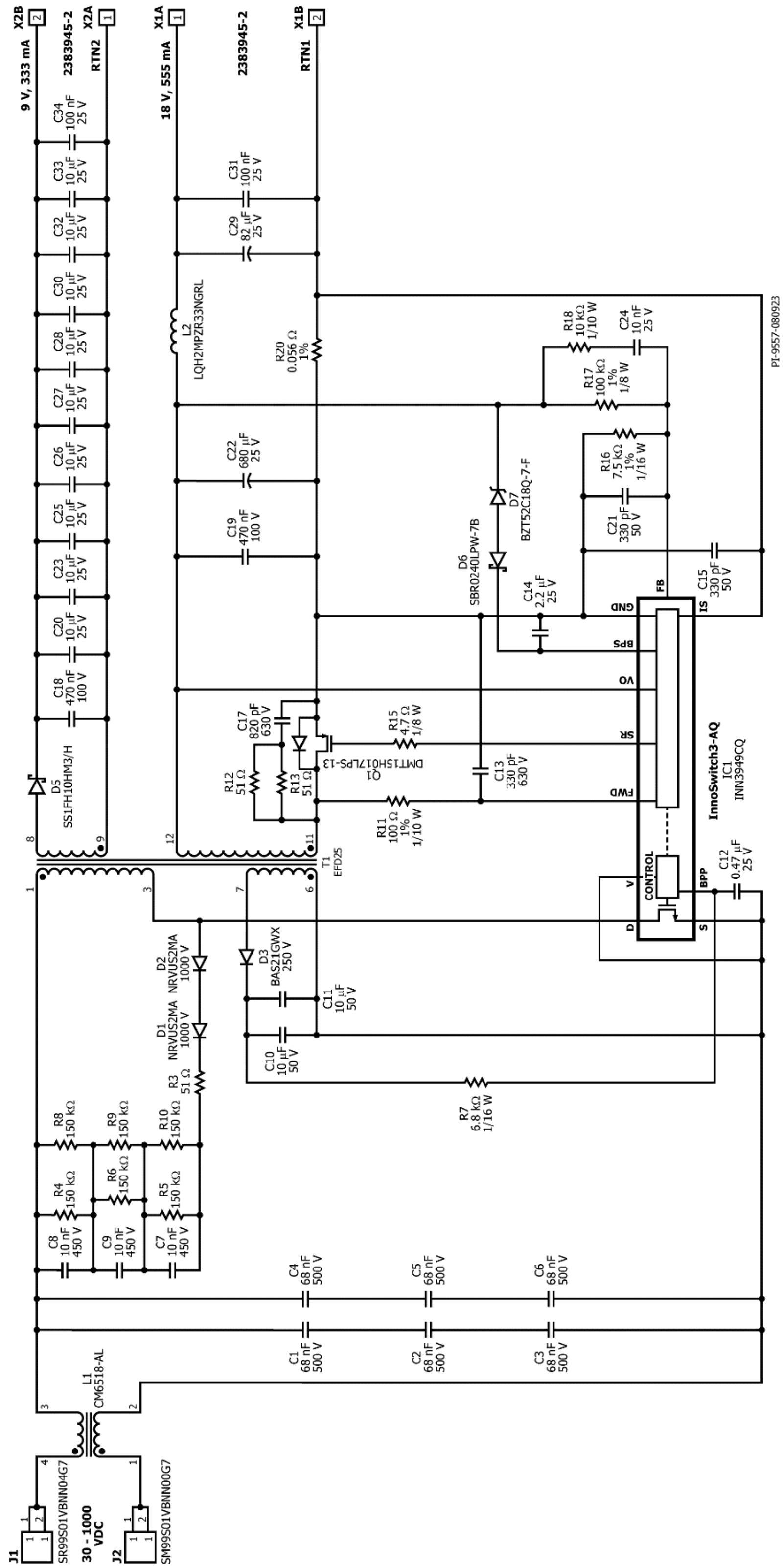

Figure 5 – DER-956Q Schematic.

4 Circuit Description

4.1 *Input Filter*

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. Large common mode currents are generated across the isolation barrier of the power supply which in turn can interfere with both the power supply operation, other inverter blocks and measurement signal integrity. The input common mode choke L1 together with the bypass capacitors C1 to C6 helps filter unwanted noise and prevents them from affecting the overall performance of the design.

Common mode inductor L1 was selected such that the reference board would be able to withstand the Power Integrations' internal "Resistance to ripple on high voltage network" test. The test injects high frequency ripple on the high voltage input to simulate the actual DC link capacitor ripple in a traction inverter. The final value of L1 will depend on the final design or application requirement. The higher the noise, the higher the inductance of L1 should be. However, consideration should be given between inductance value and the DC resistance (DCR) which has an impact on the overall efficiency of the design. Figure 6 shows how DCR of the common mode choke impacts the overall efficiency of the reference board.

Capacitor C1 to C6 bypass capacitors were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

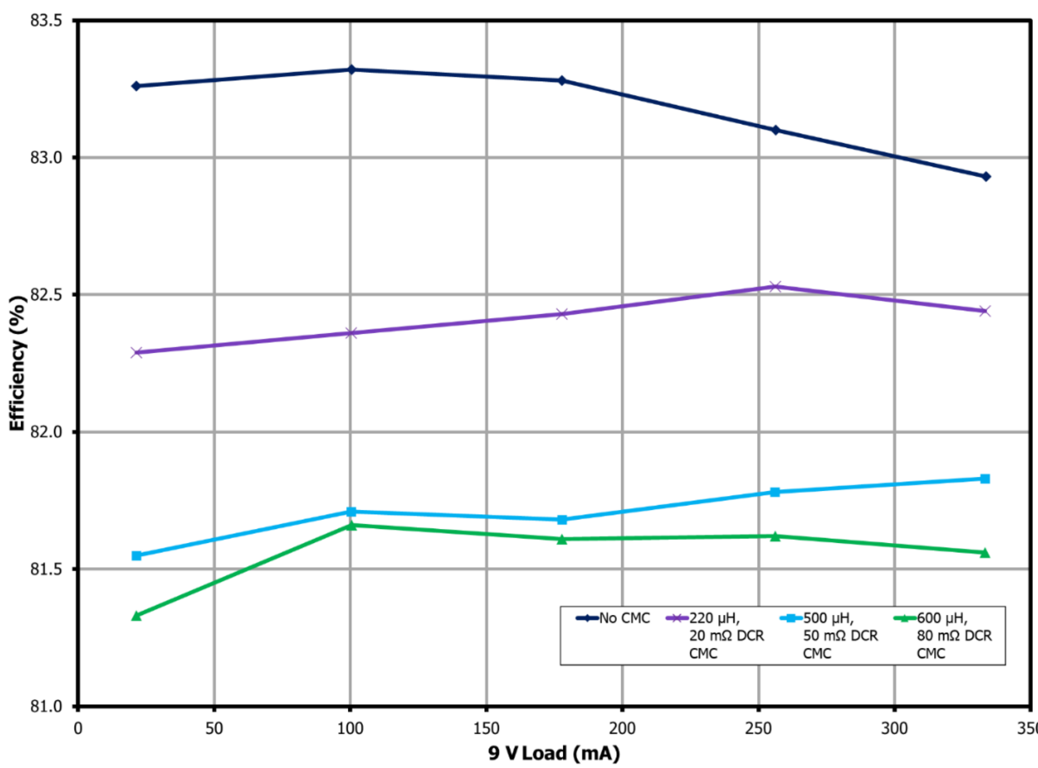

Figure 6 – DCR Effect on Efficiency at 1000 V_{DC} Input (No Input Noise) and 18 V at Maximum Load.

4.2 *High-Voltage Side Circuit*

The design uses a flyback converter to provide two isolated low voltage outputs from the high-voltage input. One end of the flyback transformer T1 primary winding is connected to the high voltage DC input while the other end is connected to the drain terminal of the integrated 1700 V power MOSFET inside the INN3949CQ IC1.

Primary clamp circuit formed by diodes D1, D2, resistors R4, R5, R6, R8, R9, R10 and capacitors C7, C8, C9 limits the peak drain-source voltage of IC1 at the instant the switch inside IC1 turns off. As compared with the traditional RCD clamp, two surface mount AEC-Q qualified diodes were used in series to meet the creepage and clearance requirements as well as to ensure that the voltage across each diode would not exceed 70% of their rating. The resistor network helps to dissipate the energy stored in the leakage reactance of transformer T1. Snubber resistors were selected such that 80% of their voltage rating would not be exceeded while maintaining power dissipation of below 50%. Cooling area for the snubber resistors were also considered to ensure operating temperature would be at acceptable level.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C12 when the DC input voltage is first applied. The INN3949CQ is guaranteed to start-up from 30 V but typically will start below this level.

During normal operation, the primary-side block is powered by the auxiliary winding of transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D3 and filtered using capacitors C10 and C11. Resistor R7 limits the BPP pin current of IC1 to a value sufficient for normal operation without incurring excessive losses.

In this design the input primary under and overvoltage features were disabled by connecting the V pin to SOURCE pin. This approach does not require the voltage sensing resistor chain used in setting the under or overvoltage feature of IC1 thus saving cost and space. However, with no undervoltage feature the output may fail to reach regulation at voltages < 40 V_{DC} with high output load current, causing the outputs to rise but fail to reach regulation (hiccup). The timing is determined by the auto-restart (AR) feature, giving a 50 ms start-up attempt followed by a 2 s off time.

If this is not acceptable on the target design or application, then the undervoltage feature can be implemented. Please refer to the datasheet for the recommended circuit and design guide.

4.3 *Low Voltage Circuit Side*

The secondary side, regulated 18 V output, of the INN3949CQ IC provides output voltage, output current sensing and gate drive for the MOSFET providing synchronous rectification (SR). The voltage across the 18 V winding of the transformer T1 is rectified by MOSFET Q1 and filtered by capacitor C19 and C22. High frequency ringing during switching is reduced by the RC snubber formed by resistors R12, R13 and capacitor C17.
Switching of Q1 is controlled by the secondary-side controller inside IC1. Control is based on the winding voltage sensed by the FWD pin via resistor R11. Capacitor C13 reduces voltage

spike on the FWD pin to ensure that voltage seen by this pin won't exceed its maximum rating of 150 V.

In continuous conduction mode operation, the primary-side power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the SR MOSFET is turned off when the voltage drop across it falls below a certain threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (via R11 and the FWD pin) or by the output voltage (via the V pin). In both cases energy is used to charge the decoupling capacitor C14 via an internal regulator.

Resistors R17 and R16 form a voltage divider network that senses the output voltage. The INN3949CQ IC has an FB pin internal reference of 1.265 V. Capacitor C21 provides decoupling from high frequency noise affecting power supply operation. C24 and R18 is a feedforward network to speed up the response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across resistor R20. The resulting current measurement is filtered with the decoupling capacitor C15 and monitored across the IS and GND pins. An internal current sense threshold of around 35 mV is used to minimize losses. Once the threshold is exceeded, the INN3949CQ IC1 will enter auto-restart (hiccup) operation until the load current is reduced below the threshold.

Similarly, the voltage across the 9 V cross regulated winding of transformer T1 is rectified by the freewheeling diode D5 and is filtered by the capacitors C18, C20, C23, C25, C26, C27, C28, C30, C32, C33. Regulation of the 9 V output depends on good coupling (low leakage inductance) to the 18 V output, this is addressed in the transformer design.

5 PCB Layout

Layers:	Six (6) (typical for traction inverter control board)
Board Material:	FR4
Board Thickness:	1.6 mm
Copper Weight:	2 oz

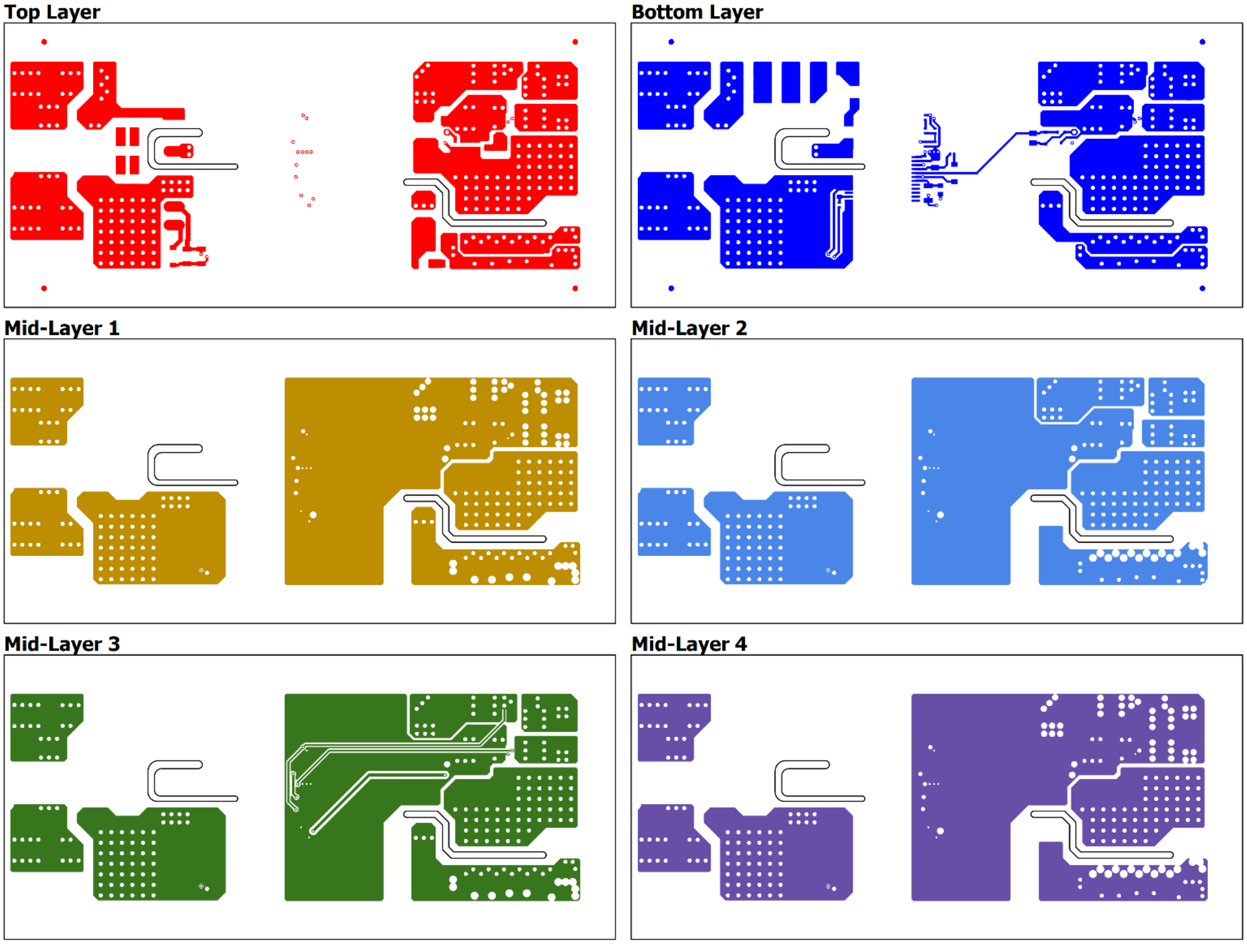

Figure 7 – DER-956Q Board Layout.

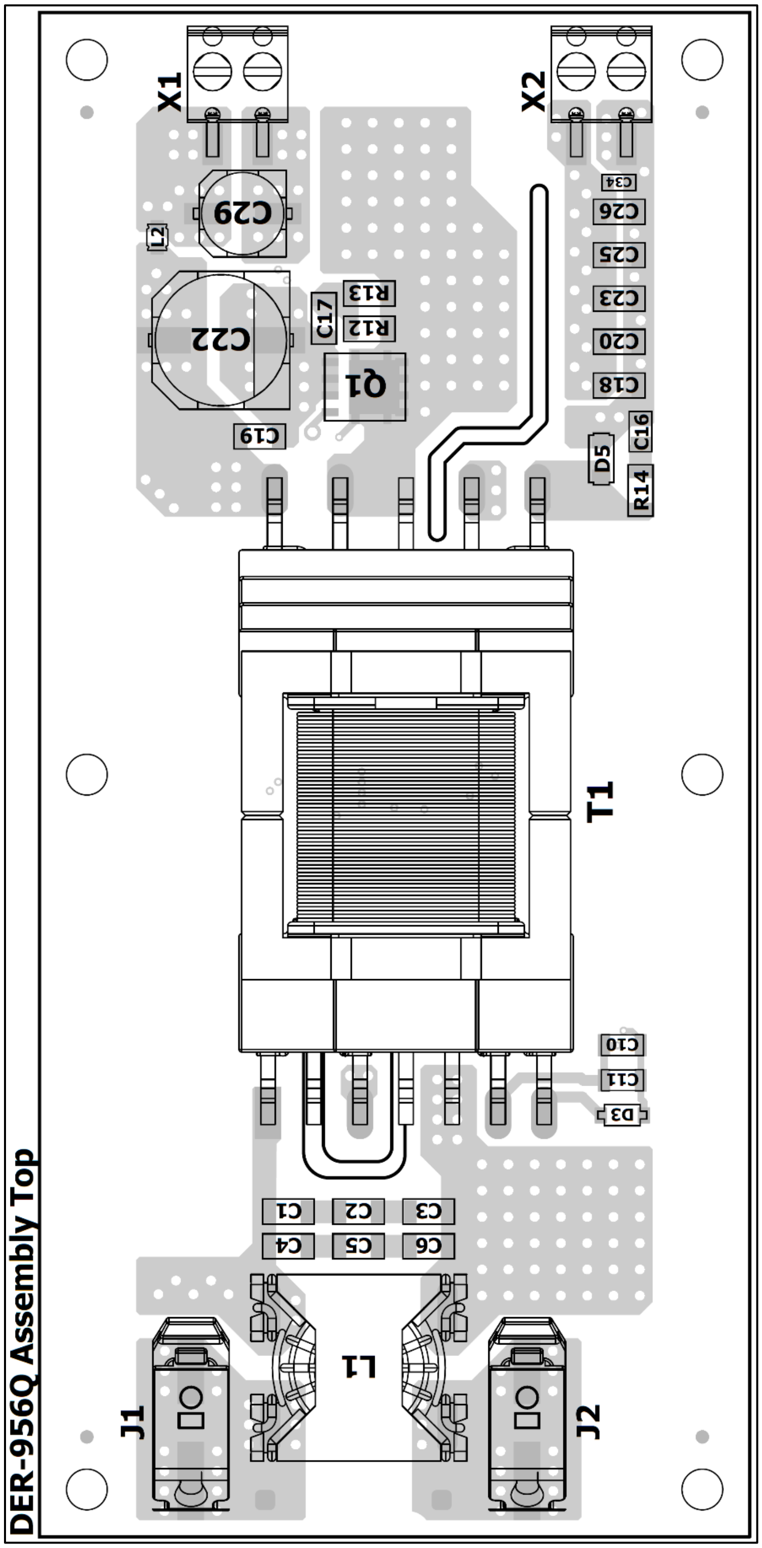

Figure 8 – DER-956Q Board Assembly (Top).

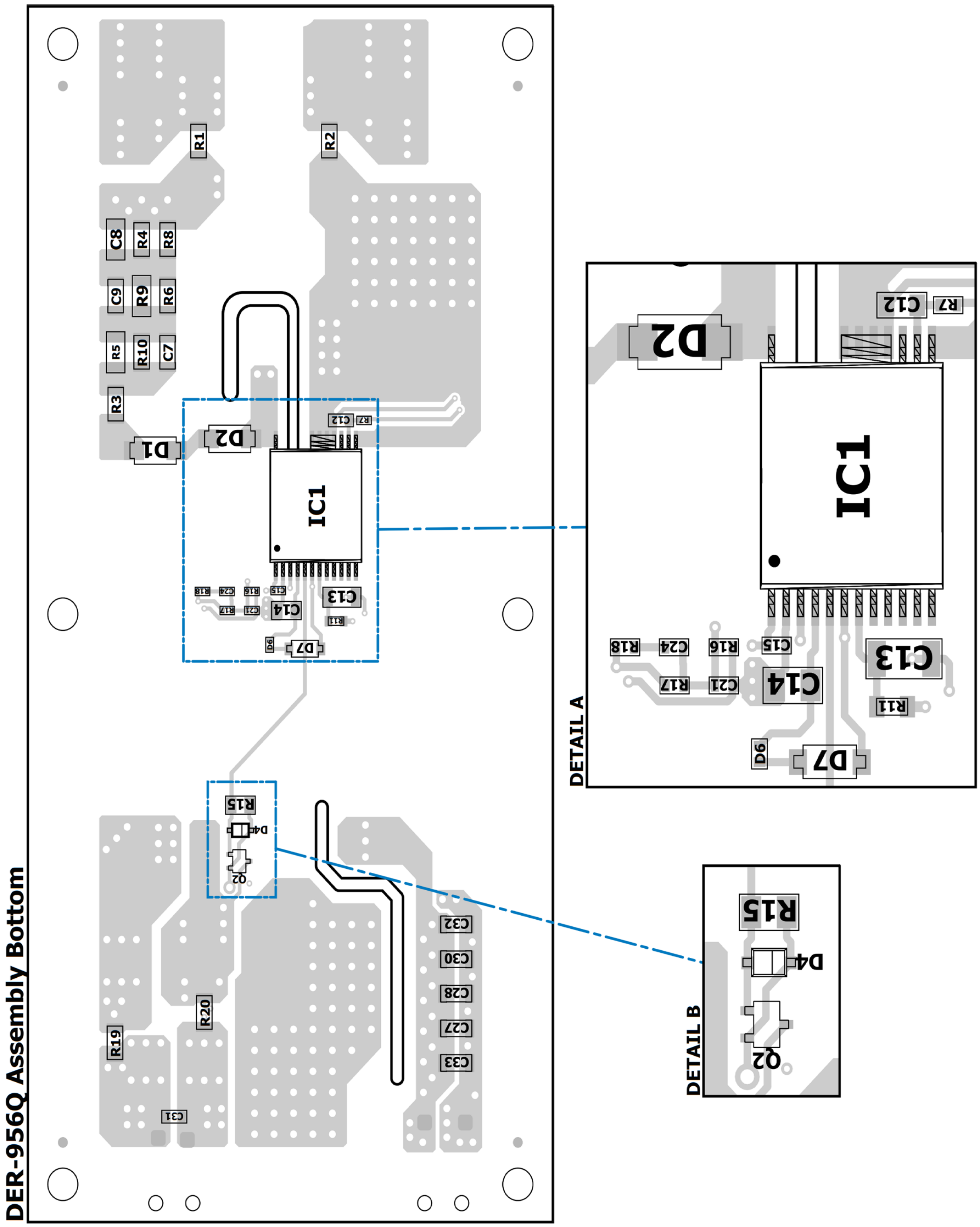

Figure 9 – DER-956Q Board Assembly (Bottom).

6 Bill of Materials

Item	Qty.	Designator	Description	MFR Part Number	Manufacturer
1	6	C1, C2, C3, C4, C5, C6	Multilayer Ceramic Capacitors MLCC - SMD/SMT 500 V 0.068 µF X7R 1206 10% AEC-Q200	C1206C683KCRACAUTO	KEMET
2	3	C7, C8, C9	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 1206 450 V 0.01 µF C0G 5% AEC-Q200	CGA5L4C0G2W103J160AA	TDK
3	2	C10, C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 50 VDC 10 µF 10% X7R AEC-Q200	CGA5L1X7R1H106K160AE	TDK
4	1	C12	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 0603 25 V 0.47 µF X7R 10% AEC-Q200	CGA3E3X7R1E474K080AB	TDK
5	1	C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 1206 630 V 330 pF C0G 5% AEC-Q200	CGA5C4C0G2J331J060AA	TDK
6	2	C15, C21	Multilayer Ceramic Capacitors MLCC - SMD/SMT 50 V 330 pF C0G 0402 5% AEC-Q200	AC0402JRNPO9BN331	YAGEO
7	1	C17	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 630 V 820 pF 5% C0G AEC-Q200	C1206C821JBGACAUTO	KEMET
8	0	C16	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0805 450 V 470 pF 5% SOFT C0G AEC-Q200	CGA4C4C0G2W471J060AE	TDK
9	1	C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0805 25 VDC 2.2 µF 10% X7R AEC-Q200	TMK212B7225KGHT	Taiyo Yuden
10	1	C22	Aluminum Organic Polymer Capacitors	EEH-ZS1E681UP	Panasonic
11	1	C24	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 0402 25 V 0.01 µF X7R 10% AEC-Q200	CGA2B2X7R1E103K050BA	TDK
12	1	C29	Aluminum Organic Polymer Capacitors	A768EB826M1ELAS036	KEMET
13	2	C31, C34	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 0603 25 V 0.1 µF X7R 10% AEC-Q200	CGA3E2X7R1E104K080AA	TDK
14	2	C18, C19	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 100 VDC 0.47 µF 10% X7R AEC-Q200	HMK316B7474KLHT	Taiyo Yuden
15	9	C20, C23, C25, C26, C27, C28, C30, C32, C33	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 25 VDC 10 µF 10% X7R AEC-Q200	CGA5L1X7R1E106K160AC	TDK
16	2	D1, D2	Rectifiers 1000 V 1.5 A High Efficiency Rectifier	NRVUS2MA	ON Semi
17	1	D3	Diodes - General Purpose, Power, Switching DIODE-GP POWER SWITCHING	BAS21GWX	Nexperia
18	0	D4	Schottky Diodes & Rectifiers 5 µA 20 Volt 15 A IFSM	SD103CWS-E3-08	Vishay
19	1	D5	Schottky Diodes & Rectifiers If 1 A Vrrm 100 V	SS1FH10HM3/H	Vishay
20	1	D6	Schottky Diodes & Rectifiers SBR Diode X1-DFN1006-2/SWP T&R 10K	SBR0240LPW-7B	Diodes, Inc.
21	1	D7	Zener Diode SOD123 T&R 3K	BZT52C18Q-7-F	Diodes, Inc.
22	1	IC1	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949CQ	Power Integrations
23	1	J1	TERM BLOCK 1POS SIDE ENTRY SMD RED	SR99S01VBNN04G7	METZ CONNECT
24	1	J2	TERM BLOCK 1POS SIDE ENTRY SMD BLACK	SM99S01VBNN00G7	METZ CONNECT
25	1	L1	Input Common Mode Choke	CM6518-AL	Coilcraft
26	1	L2	Fixed Inductors 0806 0.33 µH 30% 2200 mA 0.18 Ω	LQH2MPZR33NGRL	Murata
27	1	Q1	N-CHANNEL MOSFET BVDSS: 150 V 9.4 A 17.5 mΩ	DMT15H017LPS-13[4]	Diodes, Inc.
28	0	Q2	P-CHANNEL MOSFET BVDSS:	DMG1013UWQ-7	Diodes, Inc.
29	3	R3, R12, R13	Thick Film Resistors - SMD 51 Ω ¼ W 1206 5% AEC-Q200	AC1206JR-0751RL	YAGEO
30	0	R14	Thick Film Resistors - SMD 51 Ω ¼ W 1206 5% AEC-Q200	AC1206JR-0751RL	YAGEO
31	6	R4, R5, R6, R8, R9, R10	Thick Film Resistors - SMD 1206 150 kΩ 5% AEC-Q200	ERJ-8GEYJ154V	Panasonic
32	1	R7	Thick Film Resistors - SMD 1/16 W 6.8 kΩ 5%	CRCW04026K80JNED	Vishay
33	1	R11	Thick Film Resistors - SMD 100 Ω 100 mW 0603 1% AEC-Q200	AC0603FR-13100RL	YAGEO

[4] DMT15H017LPS-13 is qualified for AEC-Q101 reliability test only but not fully qualified for all AEC-Q criteria.

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34	1	R15	Thick Film Resistors - SMD 4.7 Ω 1/8 mW 0805 5% AEC-Q200	AC0805JR-074R7L	YAGEO
35	1	R16	Thick Film Resistors - SMD 7.5 kΩ 62.5 mW 0402 1% AEC-Q200	AC0402FR-077K5L	YAGEO
36	1	R17	Thick Film Resistors - SMD 0.125 W 100 kΩ 1% 200ppm Anti-Surge	SG73S1ETTP1003F	KOA
37	1	R18	Thick Film Resistors - SMD 0402 5% 10 kΩ Anti-Sulfur AEC-Q200	ERJ-U02J103X	Panasonic
38	1	R20	Current Sense Resistors - SMD 0.056 Ω 1% 1/4 W	RL1206FR-070R056L	YAGEO
39	2	R1, R2, R19	Thick Film Resistors - SMD 0 Ω 250 mW (1/4 W) 1206 1%	AF1206JR-070RL	YAGEO
40	1	T1	13 W Power Transformer		Power Integrations
41	1	T1-Core	3C95 Ferrite Core		Ferroxcube
42	1	T1-Bobbin	Customized bobbin		Power Integrations
43	2	X1, X2	TERMI-BLOK SMD MOUNT 180_2P_3.81	2383945-2	TE
44	1	Z1	Printed Circuit Board, PIA-00075-TL		Power Integrations

Table 4 – DER-956Q Bill of Materials[5].

[5] All components are AEC-Q qualified except for connectors, T1 and L1.

7 Transformer Specification

7.1 *Electrical Diagram*

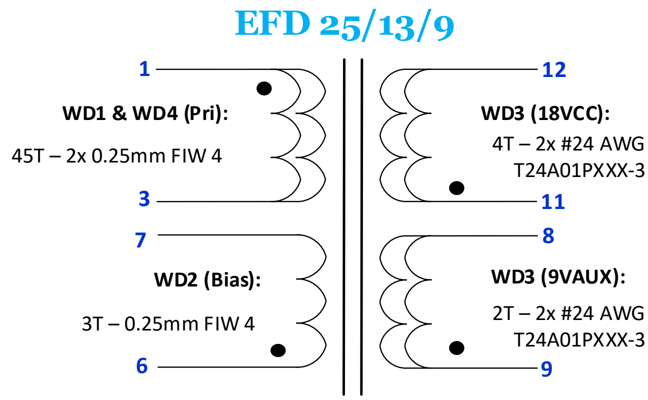


Figure 10 – Transformer Electrical Diagram.

7.2 *Electrical Specification*

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			13	W
Input Voltage Vdc	Flyback topology	30	800	1000	V
Switching Frequency	Flyback topology	25		56	kHz
Duty Cycle	Flyback topology	1.8		65.2	%
Np:Ns			11.25		
Rdc	WD1 (Pri)			390	mΩ
	WD2 (Bias)			170	
	WD3a (18 VCC)			11	
	WD3b (9 VAUX)			8	
	WD4 (Pri)			460	
Coupling Capacitance	Primary side to bias side, Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 7, with pins 1 - 3 shorted and pins 6 - 7 shorted at 25 °C			20	pF
	Primary side to 18 VCC (Sec 1) side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 12, with pins 1 - 3 shorted and pins 11 - 12 shorted at 25 °C			35	
	Primary side to 9 VAUX (Sec 2) side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 8, with pins 1 - 3 shorted and pins 8 - 9 shorted at 25 °C			20	
Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		445		μH
Part to Part Tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary Leakage Inductance	Measured at 1 V pk-pk, 100 kHz frequency between pin 1 to pin 3, with all other Windings shorted.			7.5	μH

Table 5 – Transformer electrical specification.

7.3 *Transformer Build Diagram*

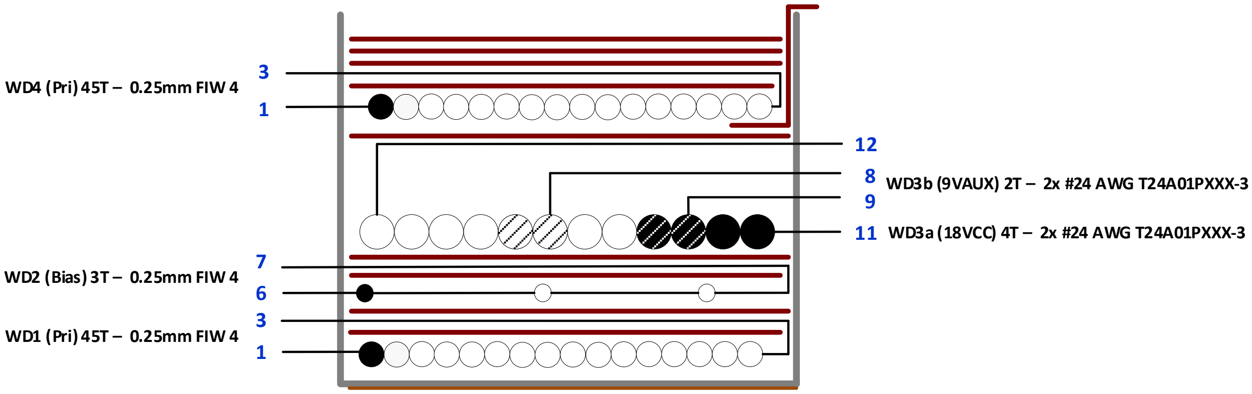


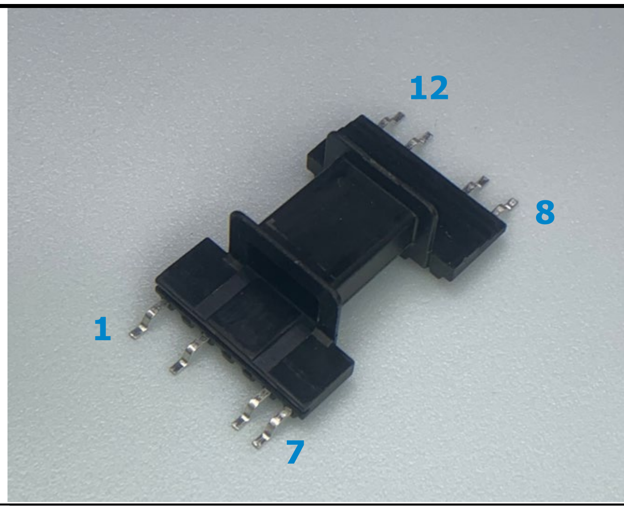
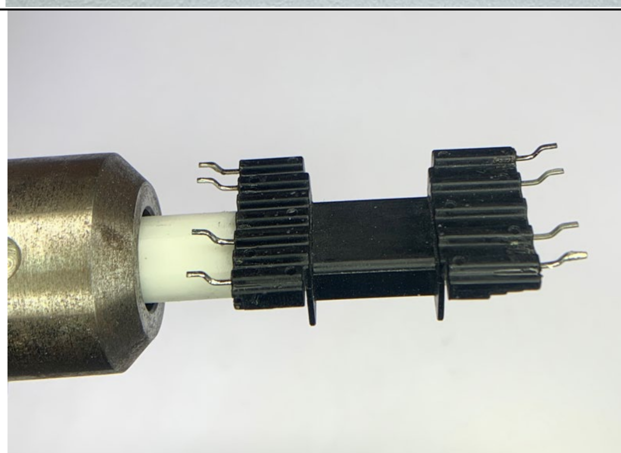
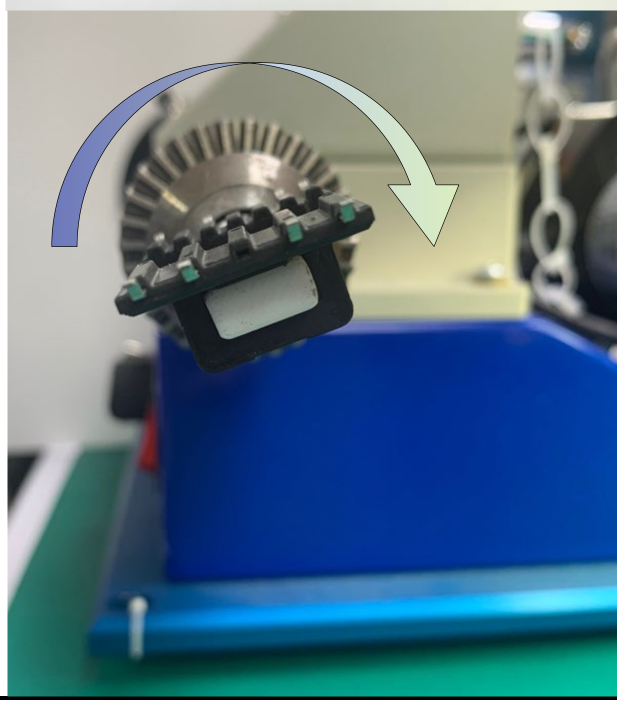
Figure 11 – Transformer Build Diagram.

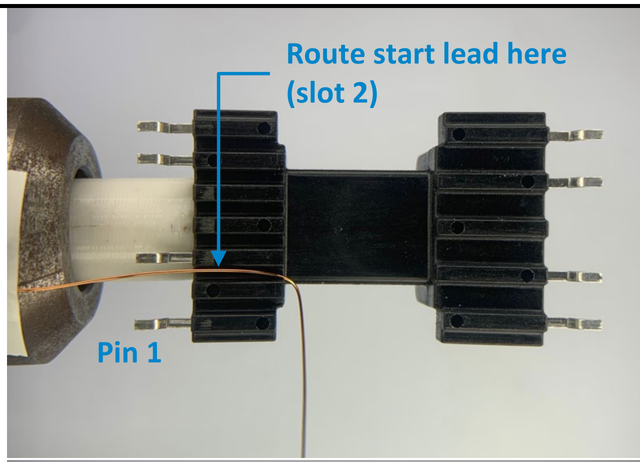
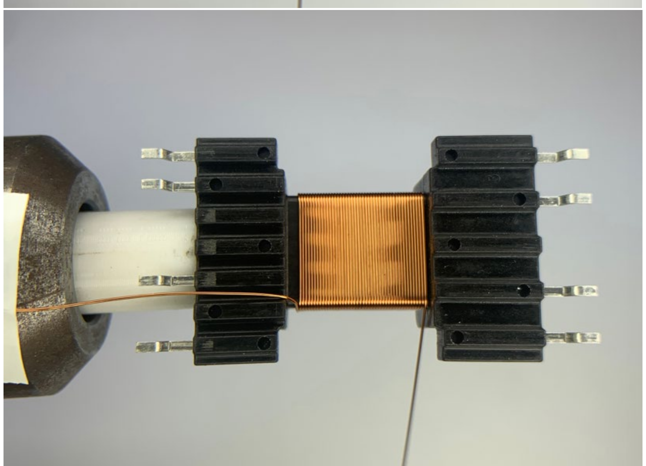
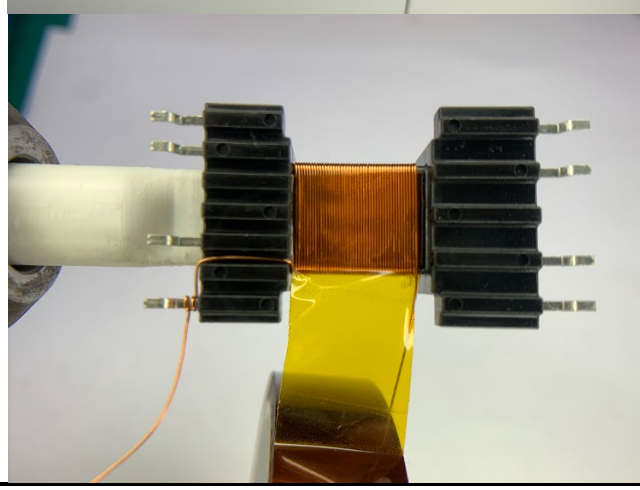
7.4 *Material List*

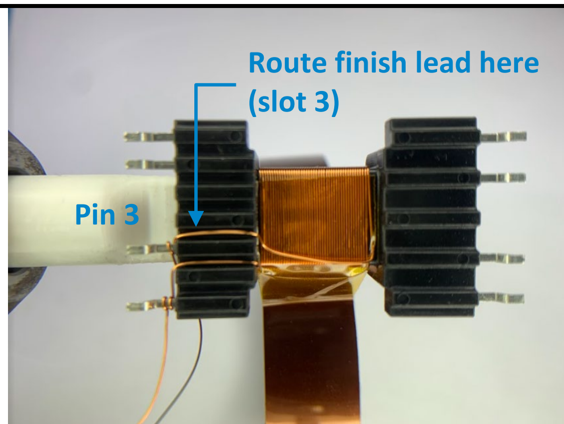
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-EFD25-N2 H7+5P	1	PC	Phenolic	MyCoilTech
[2]	Core: EFD 25/13/9	2	PCS	3C95 (or equivalent)	Ferroxcube
[3]	WD1 (Pri): 0.25 mm FIW 4, Class F	2000	mm	Copper Wire	Elektrisola
[4]	WD4 (Pri): 0.25 mm FIW 4, Class F	2310	mm		Elektrisola
[5]	WD2 (Bias): 0.25 mm FIW 4, Class F	176	mm		Elektrisola
[6]	WD3a (18 VCC): T24A01PXXX-3, AWG 24 PFA .003”	500	mm		Rubadue
[7]	WD3b (9 VAUX): T24A01PXXX-3, AWG 24 PFA .003”	320	mm		Rubadue
[8]	3M Polyimide 5413 Amber, width: 0.625in (15.9mm)	360	mm	3M157181 (or equivalent)	3M
[9]	0.51mm Teflon Tubing Class B	30	mm	TFT20024 (or equivalent)	Alphawire

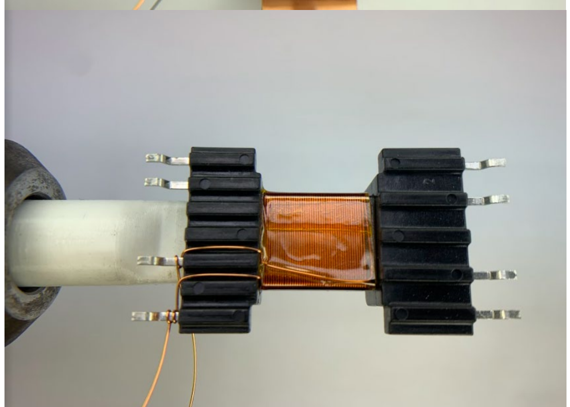
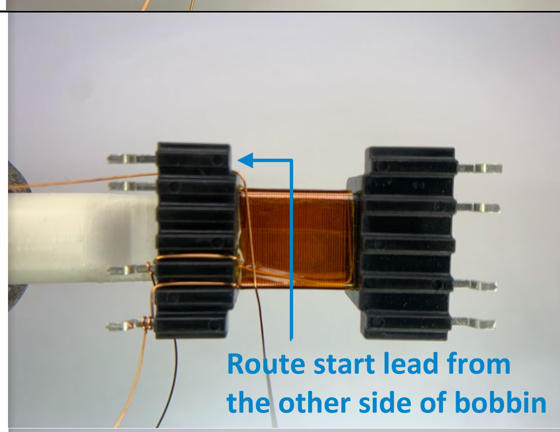
Table 6 – Transformer Bill of Materials.

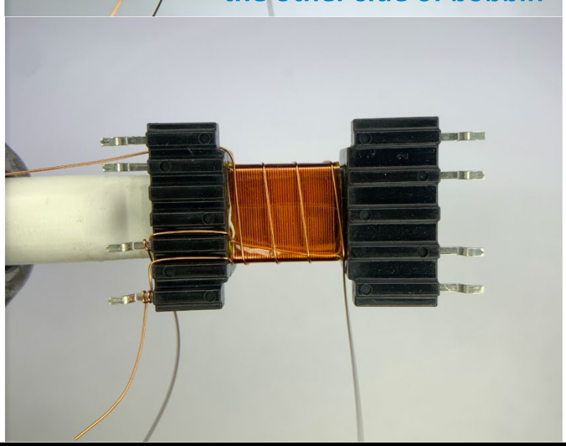
7.5 *Winding Illustrations*

Winding Preparation		Start by removing the unused pins 2, 4, 5 and 10 of the bobbin (Item [1])
	 	Position the bobbin on the mandrel such that the primary side (pins 1-7) of the bobbin is on the left side. Winding direction is clockwise direction.

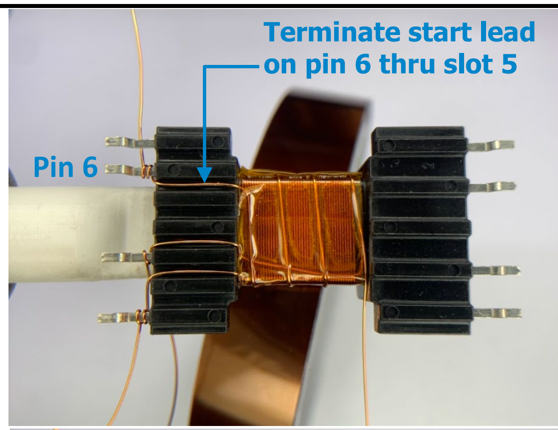
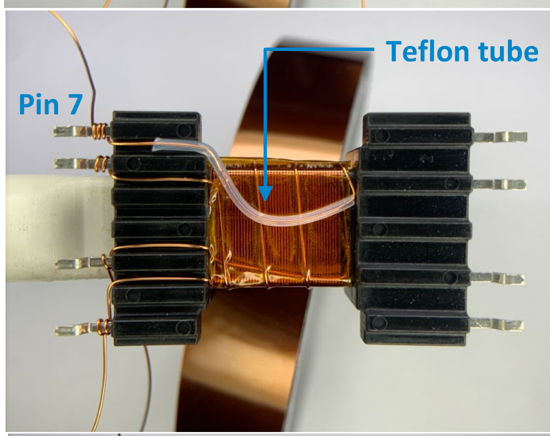
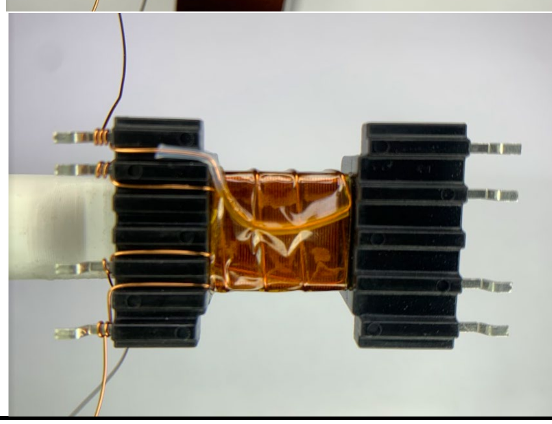
WD1: Pri	  	Route the start lead from pin 1 going to the bobbin thru slot 2 and then wind 45 turns of wire Item [3] with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Place 1 layer of tape (Item [8]) between the winding and the finish lead before terminating the finish lead to pin 3. Route the finish lead on slot 3 going to pin 3.

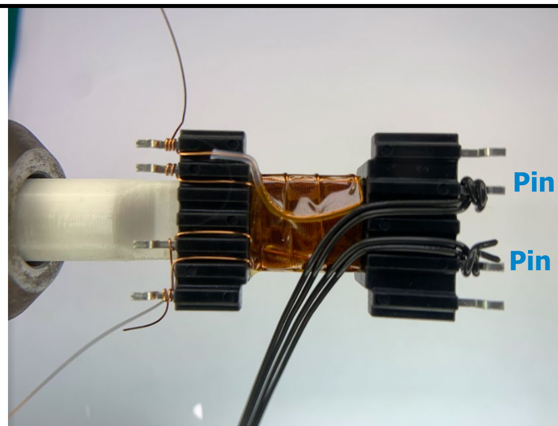
<table>
<tr>
<td></td>
<td>

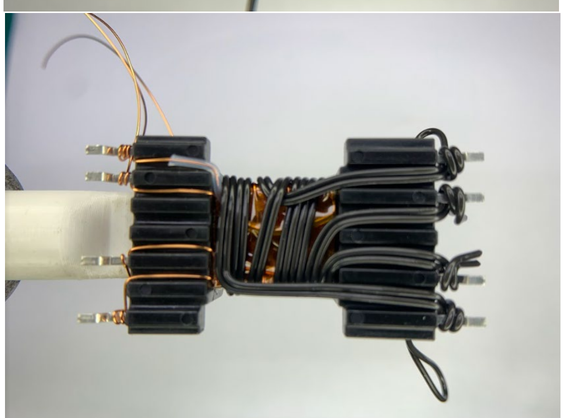
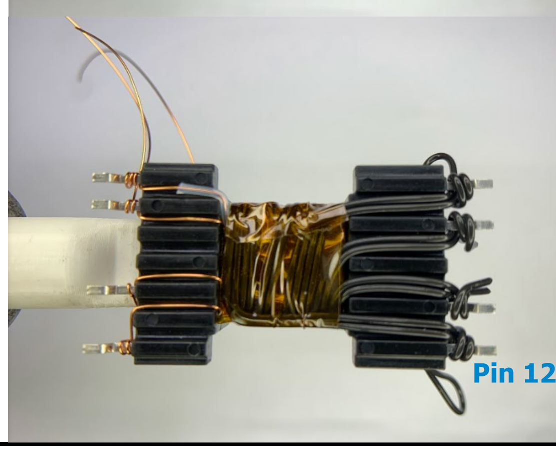
</td>
<td></td>
</tr>
<tr>
<td>WD2: Bias</td>
<td>

</td>
<td>In order to make the winding rest flat on the bobbin winding area, route the start lead initially coming from the other side of the bobbin.

Wind 3 turns of wire Item [5] with tight tension, from left to right. Spread the winding evenly along the bobbin's width.</td>
</tr>
</table>

	  	Place 1 layer of tape (Item [8]) between the winding and the finish lead. Before closing the layer of tape, terminate the start lead on Pin 6 and insert teflon tube Item [9] on the finish lead then terminate it to pin 7.

<table>
<tr>
<td>WD3: 18 VCC and 9 VAUX</td>
<td>


</td>
<td>Use 2 strands of wire Item [7] for the 9 VAUX winding and start it at pin 9.
Also use 2 strands of wire Item [6] for the 18 VCC winding and start it at pin 11.

Wind all wires together with tight tension, from right to left.

After 2 turns, fold the end of the bifilar 9 VAUX winding to the right then terminate it to pin 8 and continue to wind the 18 VCC bifilar winding for 2 more additional turns.

Place 1 layer of tape (Item [8]) to finish WD3.</td>
</tr>
</table>

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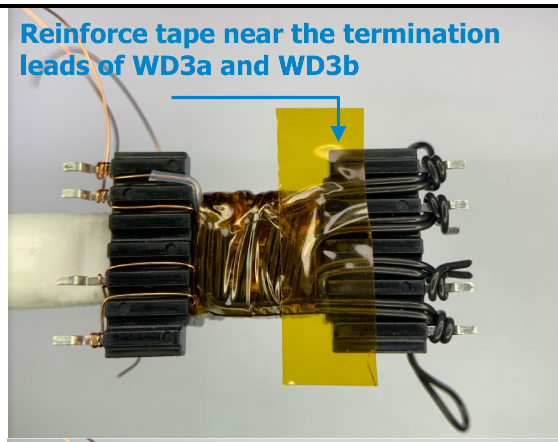
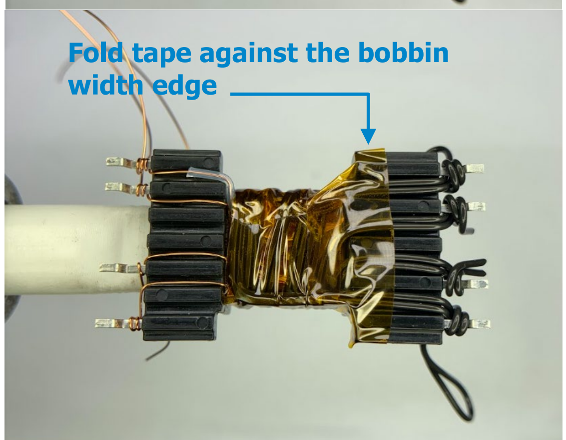
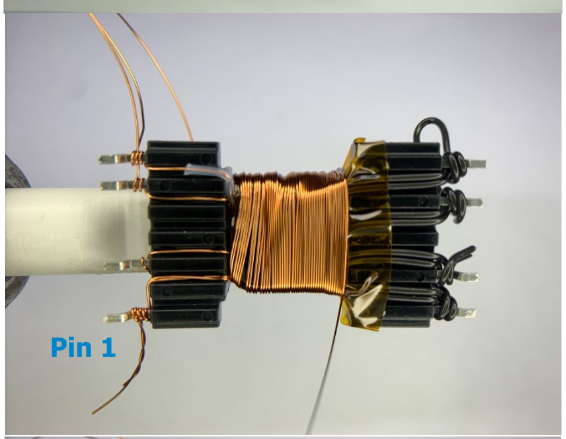
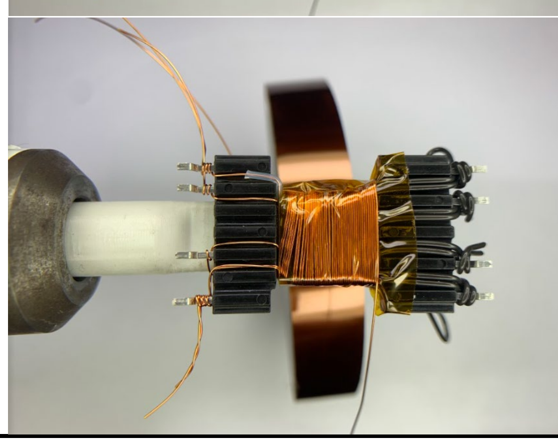
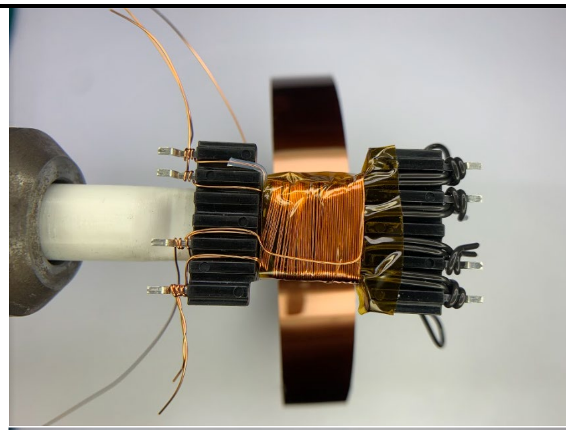
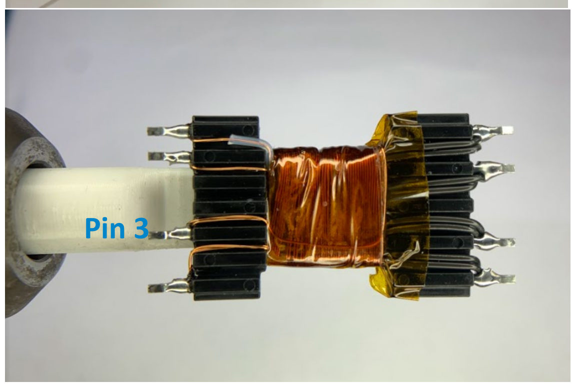
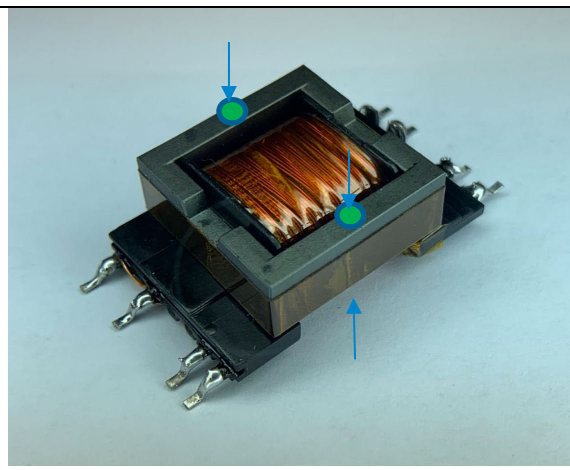
WD4: Pri	   	Before winding WD4, reinforce the insulation near the termination end of WD3 by placing 1 layer of tape (Item [8]) as shown. Trim the reinforced tape and fold it flat against the bobbin width edge as shown. Start at pin 1, wind 45 turns of wire Item [4] with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Place 1 layer of tape (Item [8]) between the winding and the finish lead before terminating the finish lead to pin 3.

	  	Finish up by placing 3 layers of tape (Item [8]). Solder all terminated pins (pin 1, 3, 6, 7, 8, 9, 11 and 12).
Finishing		Gap one of the core halves (item [2]) and fasten the core tightly to get 445 µH ± 5% of inductance between pins 1 and 3. In fastening the core, it is preferred to use glue instead of tape that is used in the illustration (see blue arrows for the preferred gluing points – 2 points on top and 2 points on the bottom.)

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ _Flyback_012722; Rev.3.2; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VOUT	18.00		18.00	V	Output Voltage
4	OPERATING CONDITION 1					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	0.722		0.722	A	Output current 1
7	POUT1			13.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	OPERATING CONDITION 2					
12	VINDC2	450.00		450.00	V	Input DC voltage 2
13	IOUT2	0.722		0.722	A	Output current 2
14	POUT2			13.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	PRIMARY CONTROLLER SELECTION					
70	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
71	VDRAIN_BREAKDOWN			1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.900	A	Primary switch typical current limit
79	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.03	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1230	V	Peak drain voltage on the primary switch during turn-off
85	WORST CASE ELECTRICAL PARAMETERS					
86	FSWITCHING_MAX	33000		33000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	200.0		200.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			9.413		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.045		Primary switch duty cycle
91	TIME_ON_MIN			0.60	us	Minimum primary switch on-time
92	TIME_ON_MAX			1.56	us	Maximum primary switch on-time
93	TIME_OFF			28.97	us	Primary switch off-time
94	LPRIMARY_MIN			422.5	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			444.7	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			467.0	uH	Maximum primary magnetizing inductance
99	PRIMARY CURRENT					
100	IAVG_PRIMARY			1.540	A	Primary switch average current
101	IPEAK_PRIMARY			1.540	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.031	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.540	A	Primary switch ripple current
104	IRMS_PRIMARY			0.180	A	Primary switch RMS current
108	TRANSFORMER CONSTRUCTION PARAMETERS					
109	CORE SELECTION					

110	CORE	CUSTOM		CUSTOM		Core selection
111	CORE NAME	EFD 25/13/9-3C95		EFD 25/13/9-3C95		Core code
112	AE	58.0		58.0	mm^2	Core cross sectional area
113	LE	57.0		57.0	mm	Core magnetic path length
114	AL	2660		2660	nH	Ungapped core effective inductance per turns squared
115	VE	3300		3300	mm^3	Core volume
116	BOBBIN NAME	MCT-EFD25-N2 H7+5P		MCT-EFD25-N2 H7+5P		Bobbin name
117	AW	38.5		38.5	mm^2	Bobbin window area
118	BW	16.20		16.20	mm	Bobbin width
119	MARGIN			0.0	mm	Bobbin safety margin
121	**PRIMARY WINDING**					
122	NPRIMARY			45		Primary winding number of turns
123	BPEAK			3723	Gauss	Peak flux density
124	BMAX			2689	Gauss	Maximum flux density
125	BAC			1344	Gauss	AC flux density (0.5 x Peak to Peak)
126	ALG			220	nH	Typical gapped core effective inductance per turns squared
127	LG			0.304	mm	Core gap length
129	**SECONDARY WINDING**					
130	NSECONDARY			4		Secondary winding number of turns
132	**BIAS WINDING**					
133	NBIAS			3		Bias winding number of turns
137	**PRIMARY COMPONENTS SELECTION**					
138	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
139	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
140	UNDERVOLTAGE PARAMETERS					
141	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
142	UNDERVOLTAGE ZENER DIODE	BZM55C9 V1		BZM55C9 V1		Undervoltage protection zener diode
143	VZ			9.10	V	Zener diode reverse voltage
144	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
145	ILKG			2.00	uA	Zener diode maximum reverse leakage current
146	BROWN-IN ACTUAL			22.99 - 29.55	V	Actual brown-in voltage range using standard resistors
147	BROWN-OUT ACTUAL			19.76 - 26.44	V	Actual brown-out voltage range using standard resistors
148	OVERVOLTAGE PARAMETERS					
149	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
150	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
151	VF				V	OV diode forward voltage
152	VRRM				V	OV diode reverse voltage
153	PIV				V	OV diode peak inverse voltage
154	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
155	**DC BUS SENSE RESISTORS**					
156	RLS_H			0.70	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
157	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
160	**BIAS WINDING**					
161	VBIAS			9.00	V	Rectified bias voltage

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162	VF_BIAS	1.00		1.00	V	Bias winding diode forward drop
163	VREVERSE_BIASDIODE			75.67	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
164	CBIAS			22	uF	Bias winding rectification capacitor
165	CBPP			0.47	uF	BPP pin capacitor
169	**SECONDARY COMPONENTS SELECTION**					
170	**FEEDBACK COMPONENTS**					
171	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
172	RFB_LOWER			7.50	kΩ	Lower feedback resistor
173	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
177	**MULTIPLE OUTPUT PARAMETERS**					
178	**OUTPUT 1**					
179	VOUT1			18.00	V	Output 1 voltage
180	IOUT1	0.555		0.555	A	Output 1 current
181	POUT1			9.99	W	Output 1 power
182	IRMS_SECONDARY1			2.330	A	Root mean squared value of the secondary current for output 1
183	IRIPPLE_CAP_OUTPUT1			2.263	A	Current ripple on the secondary waveform for output 1
184	NSECONDARY1			4		Number of turns for output 1
185	VREVERSE_RECTIFIER1			106.89	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
186	SRFET1	AUTO		DMT15H017LPS-13		Secondary rectifier (Logic MOSFET) for output 1
187	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
188	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
189	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
191	**OUTPUT 2**					
192	VOUT2	9.00		9.00	V	Output 2 voltage
193	IOUT2	0.333		0.333	A	Output 2 current
194	POUT2			3.00	W	Output 2 power
195	IRMS_SECONDARY2			1.398	A	Root mean squared value of the secondary current for output 2
196	IRIPPLE_CAP_OUTPUT2			1.358	A	Current ripple on the secondary waveform for output 2
197	NSECONDARY2			2		Number of turns for output 2
198	VREVERSE_RECTIFIER2			53.44	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
199	SRFET2	AUTO		SQSA80ENW		Secondary rectifier (Logic MOSFET) for output 2
200	VF_SRFET2			0.82	V	SRFET on-time drain voltage for output 2
201	VBREAKDOWN_SRFET2			80	V	SRFET breakdown voltage for output 2
202	RDSON_SRFET2			27.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
203						
217	PO_TOTAL			12.99	W	Total power of all outputs

Table 7 – DER-956Q PIXls Spreadsheet.

9 Performance Data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a High Voltage (HV) room.

Figure 12 – High Voltage Test Set-up.

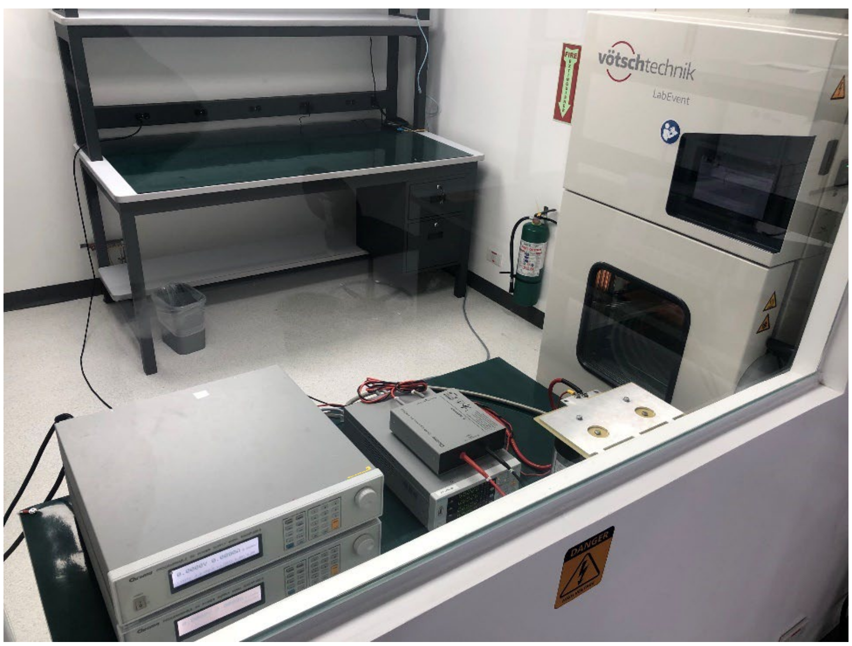


Figure 13 - Test Set-up Inside the High Voltage Room.

2. Unit under test was placed under a box while inside the thermal chamber to eliminate the effect of any airflow.

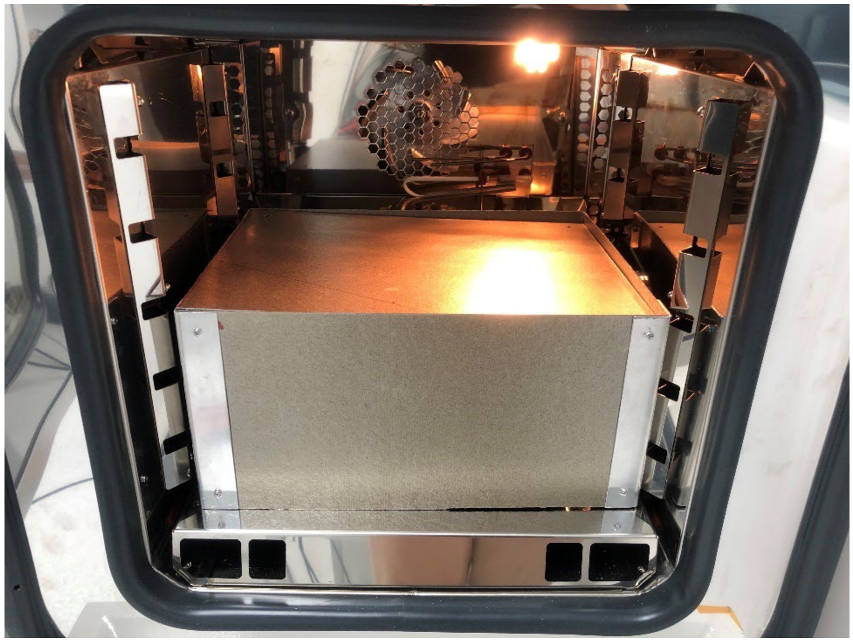


Figure 14 – Unit under test placed under a box to eliminate the effect of airflow.

3. For data points showing performance across varying input line voltages and output loading conditions, the unit under test was soaked at full load condition for at least 5 minutes for every change in the input voltage during the start of each test sequence. Also, for every loading condition, the unit under test was soaked for at least 20 seconds before measurements were taken.

9.1 *No-Load Input Power*

Figure 15 shows the test set up diagram for no load input current acquisition. The voltage metering point is placed before the ammeter; this is done to prevent the voltage sensing bias current from affecting the input current measurement. The ammeter used was Tektronix DMM 4050 6-1/2 Digit Precision Multimeter.

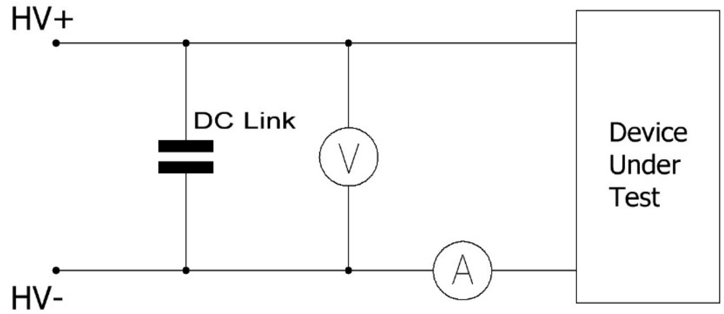


Figure 15 - No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes before starting data averaging of fifty thousand samples over a period of one minute. Analog filtering is also enabled to improve measurement accuracy.

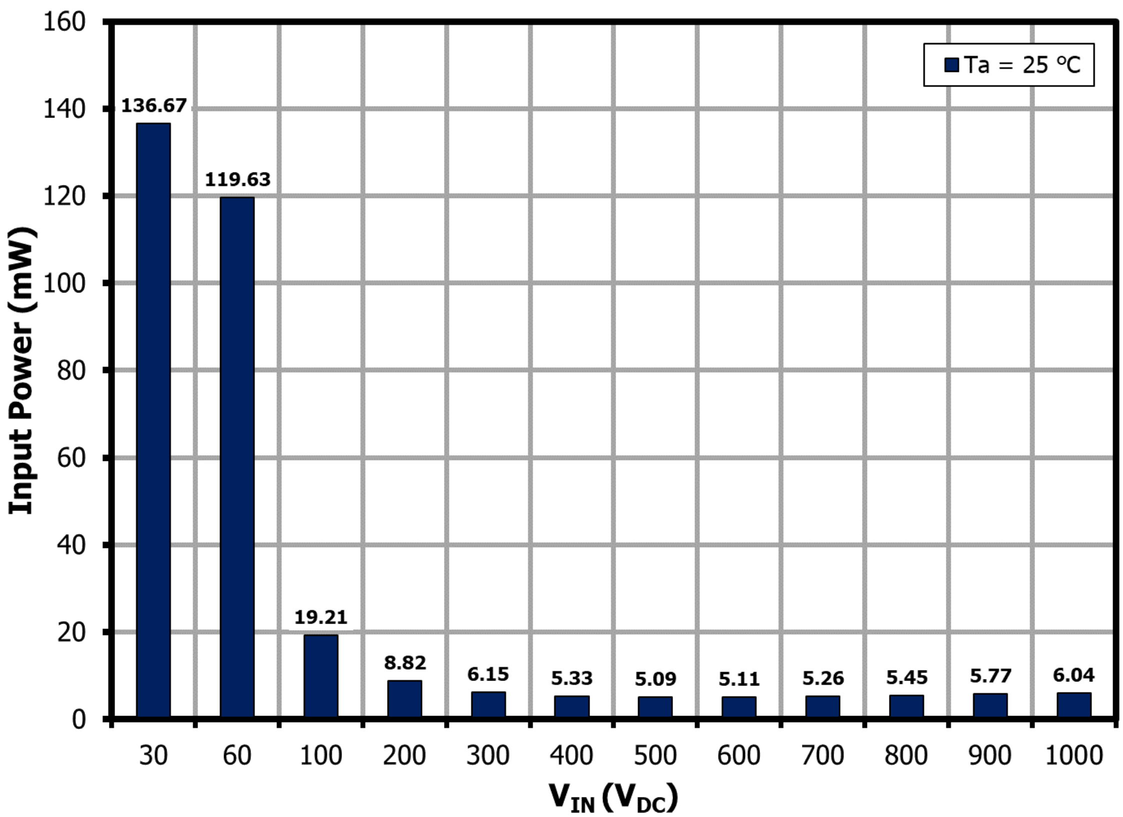


Figure 16 – No-load Input Power vs. Input Line Voltage.

9.2 *Efficiency*

9.2.1 Line Efficiency

Line efficiency describes how the change in input voltage affects the overall efficiency of the unit.

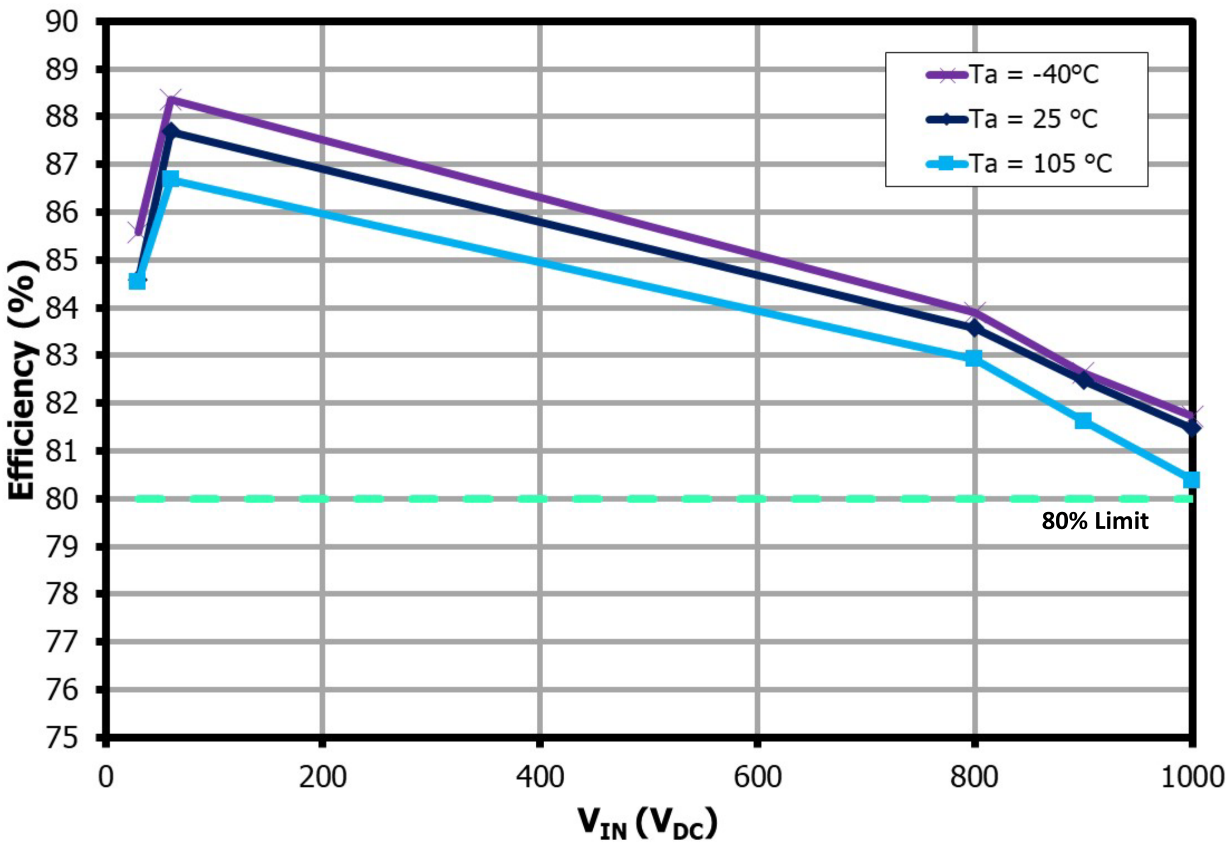


Figure 17 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the overall efficiency of the unit.
Each line on the graphs represents the efficiency vs. total output power of the unit under test when the 18V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

9.2.2.1 30 V_{DC} Input

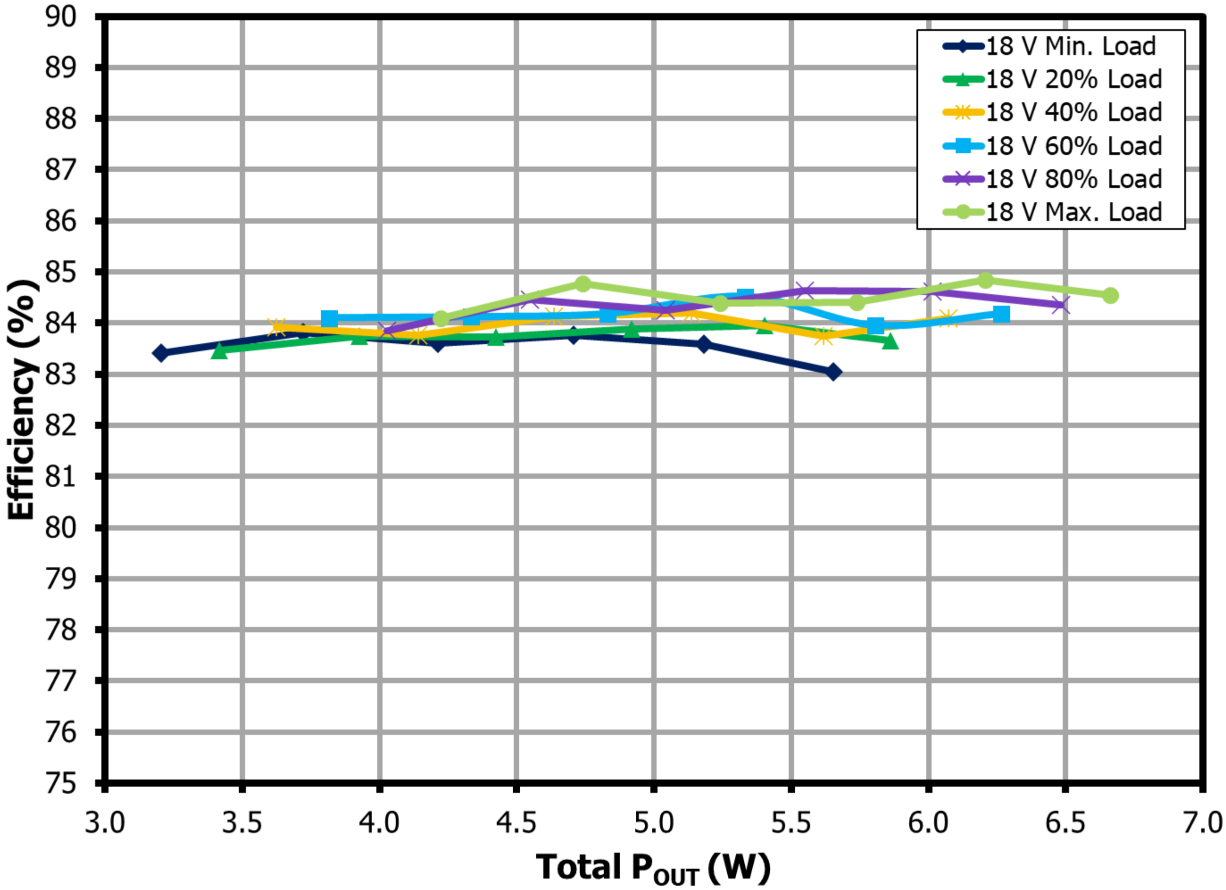


Figure 18 – Efficiency vs. Total Output Power at 30 V_{DC} Input and 105 °C Ambient Temperature.

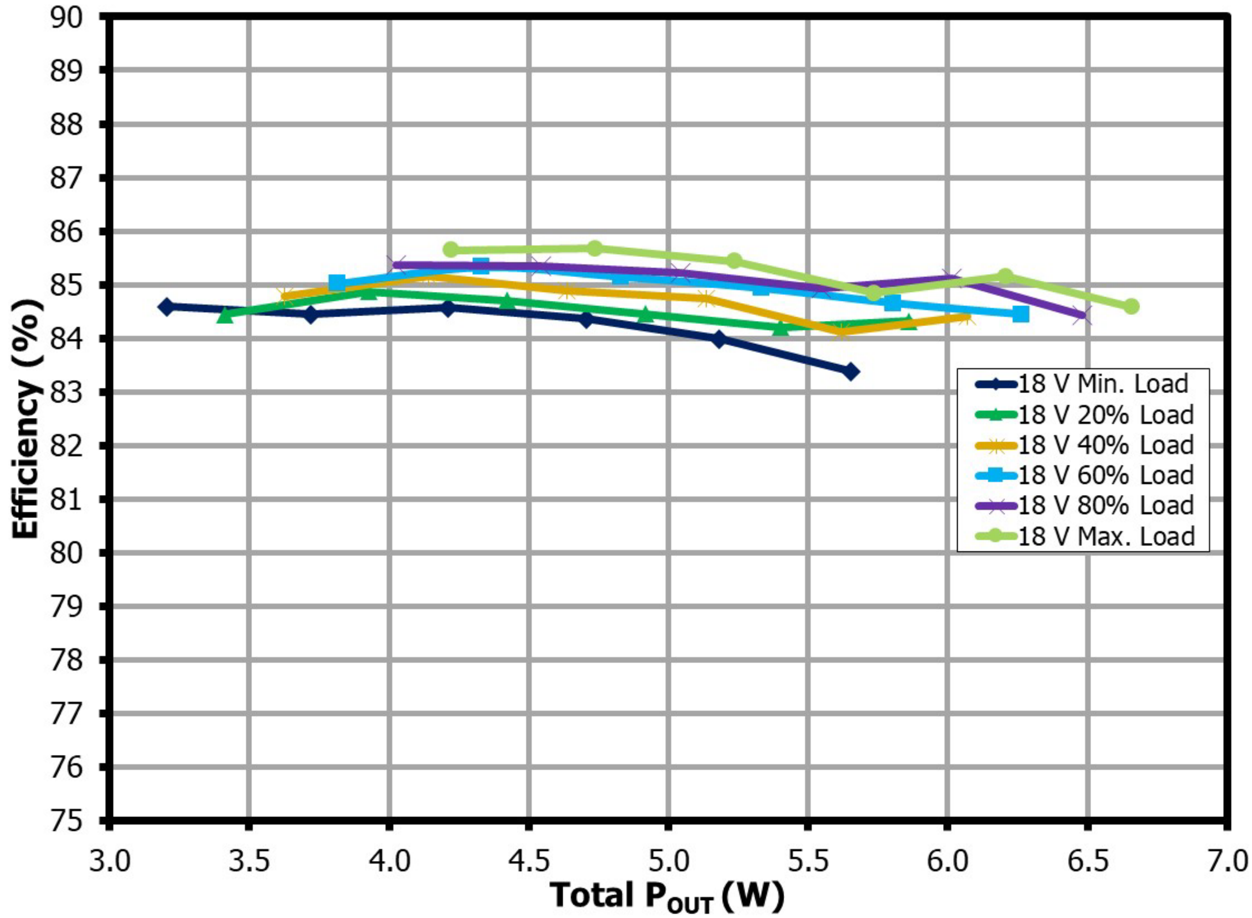


Figure 19 – Efficiency vs. Total Output Power at 30 V_{DC} Input and 25 °C Ambient Temperature.

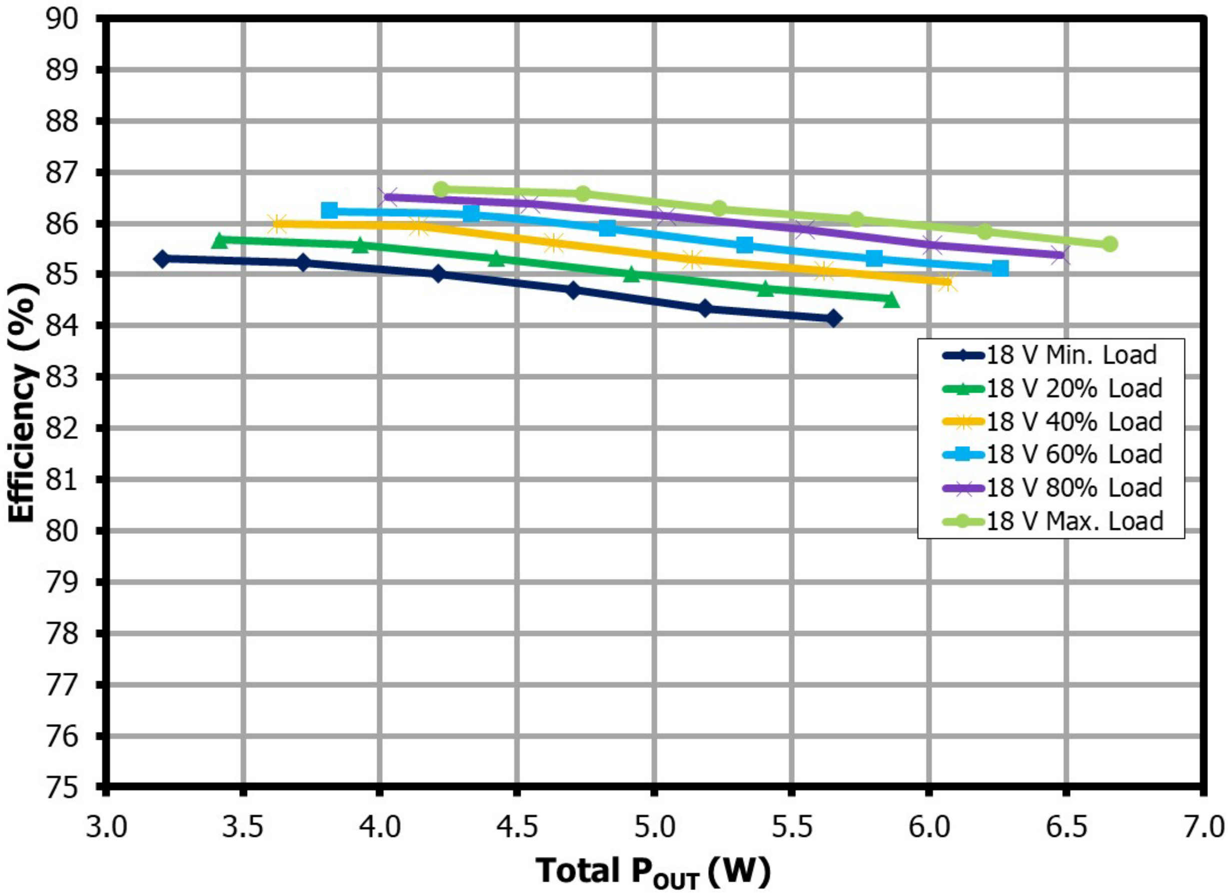


Figure 20 – Efficiency vs. Total Output Power at 30 V_{DC} Input and -40 °C Ambient Temperature.

9.2.2.2 60 V_{DC} Input

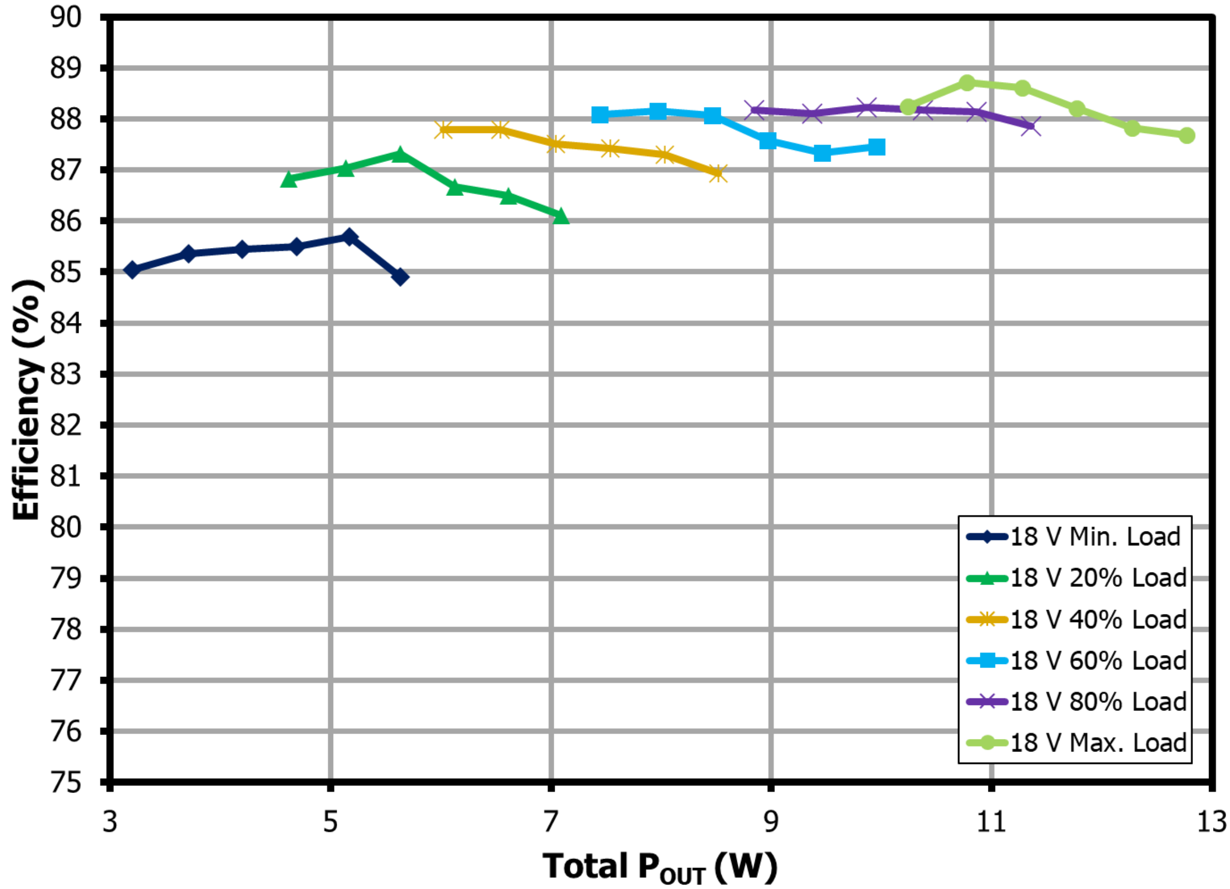


Figure 21 – Efficiency vs. Total Output Power at 60 V_{DC} Input and 105 °C Ambient Temperature.

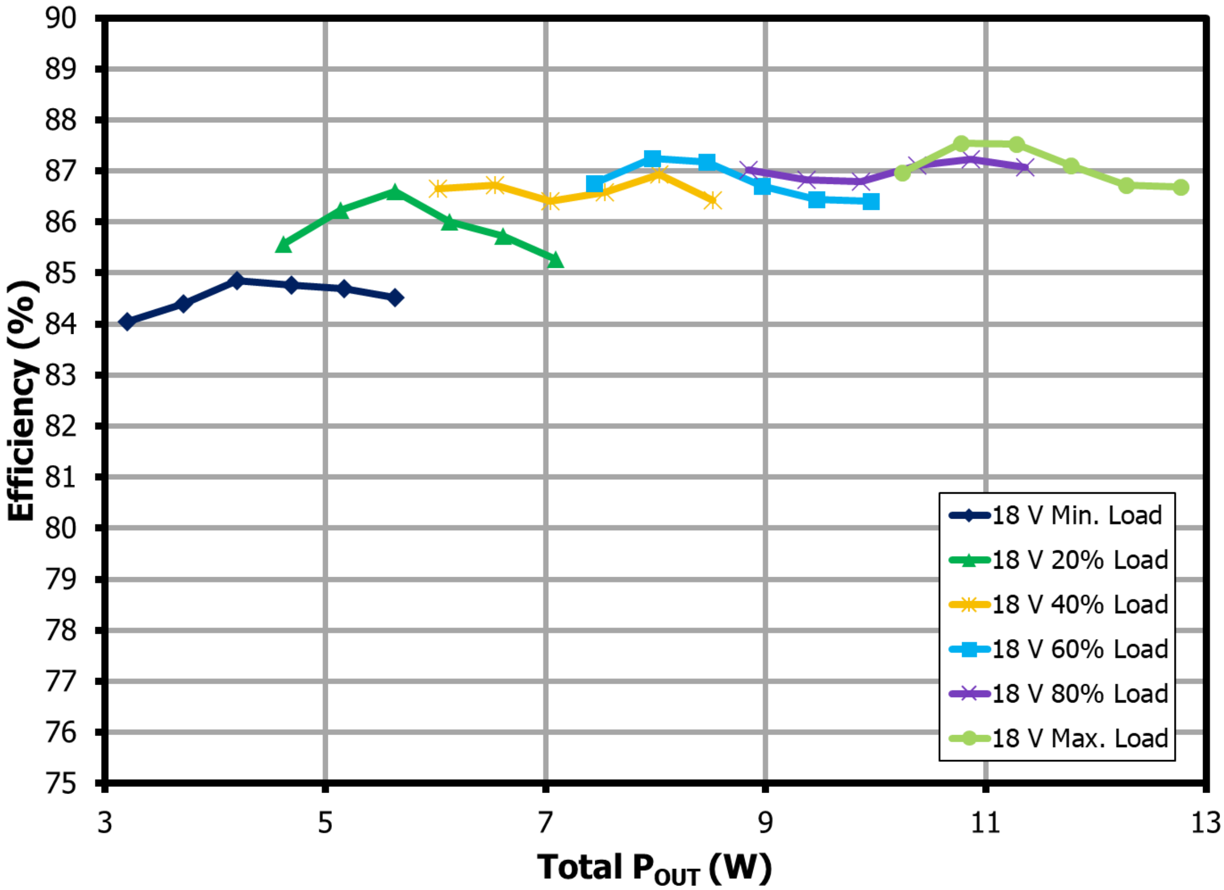


Figure 22 – Efficiency vs. Total Output Power at 60 V_{DC} Input and 25 °C Ambient Temperature.

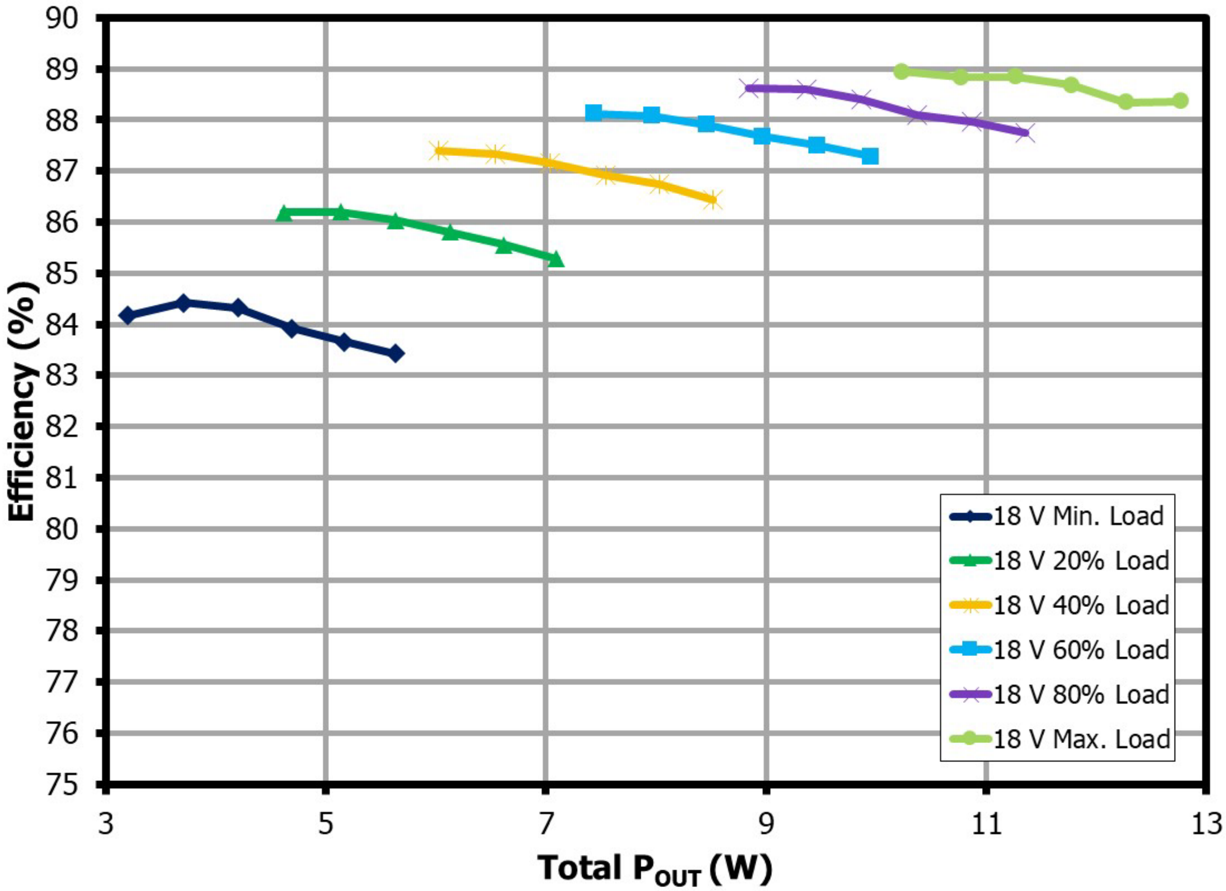


Figure 23 – Efficiency vs. Total Output Power at 60 VDC Input and -40 °C Ambient Temperature.

9.2.2.3 800 V_{DC} Input

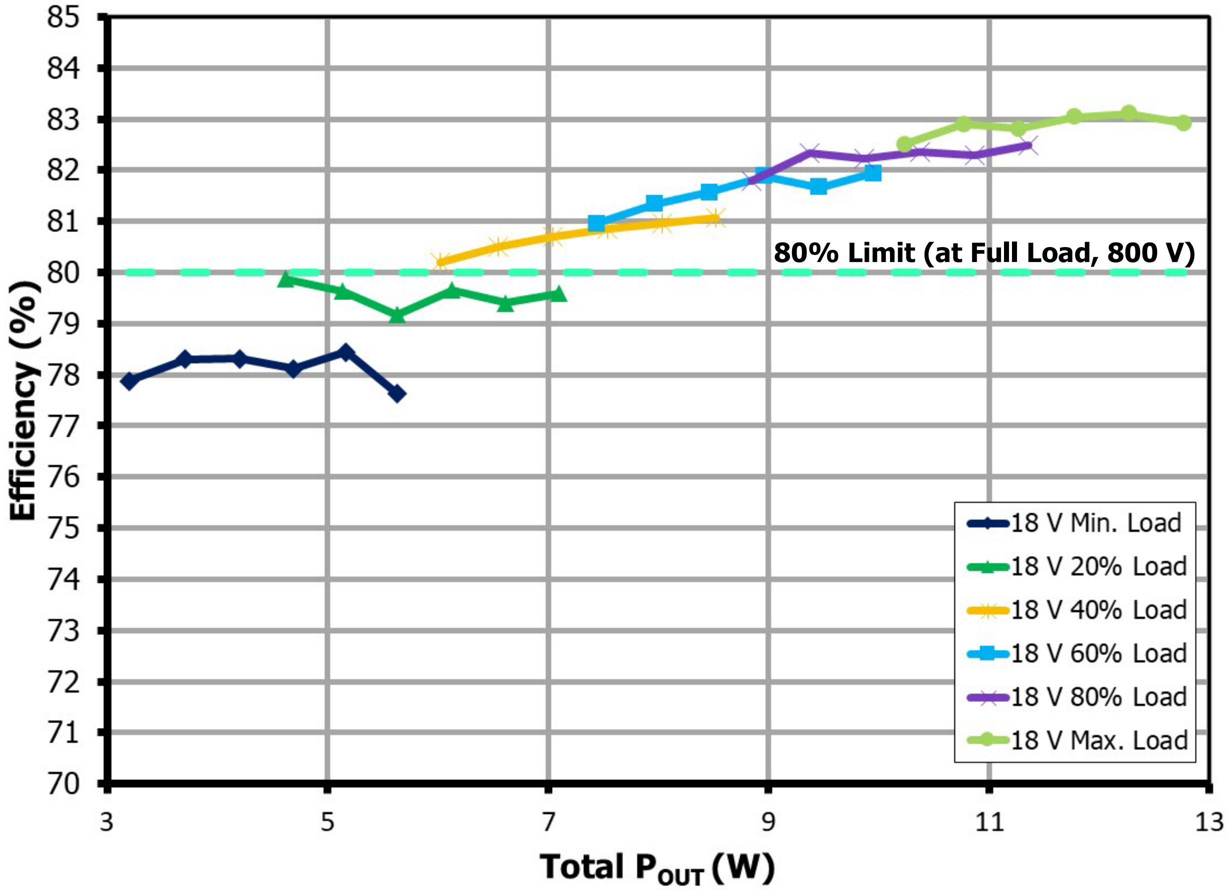


Figure 24 – Efficiency vs. Total Output Power at 800 V_{DC} Input and 105 °C Ambient Temperature.

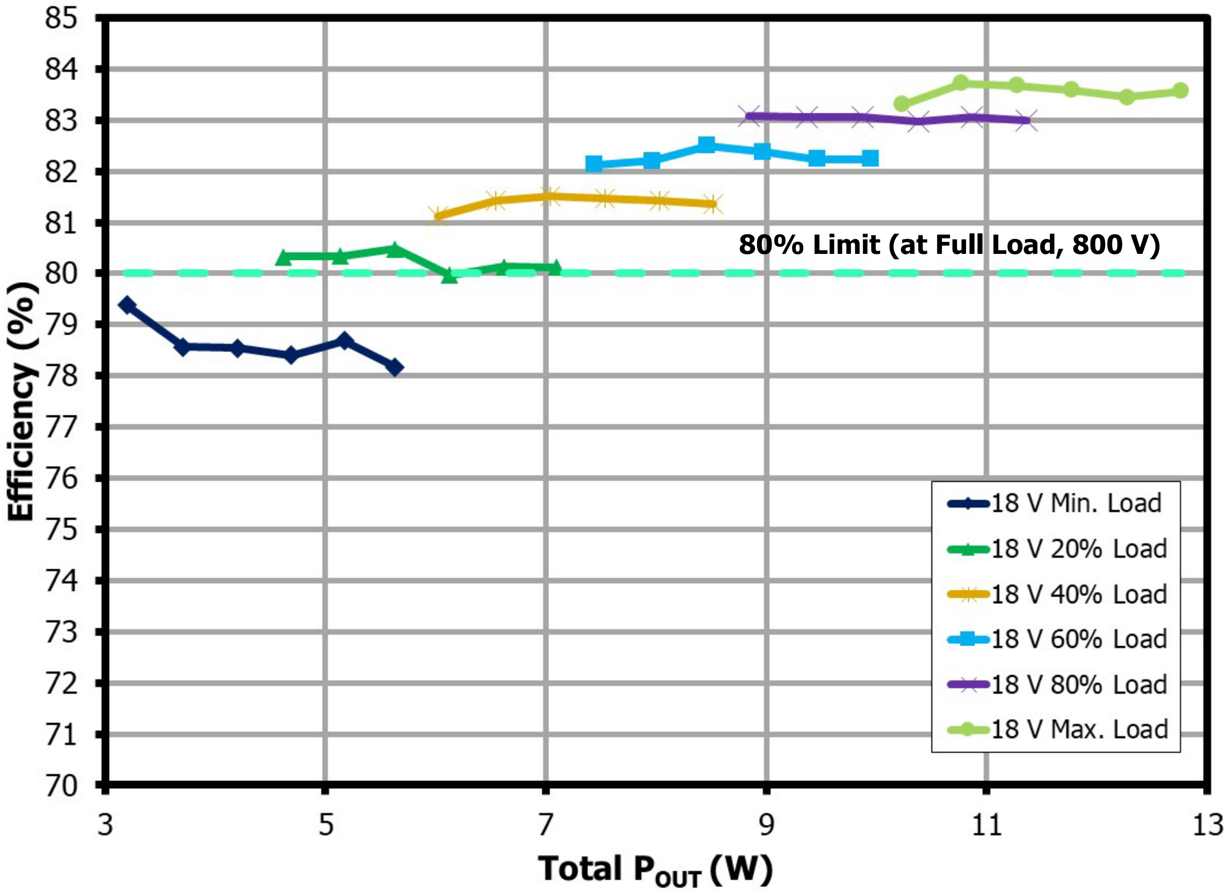


Figure 25 – Efficiency vs. Total Output Power at 800 V_{DC} Input and 25 °C Ambient Temperature.

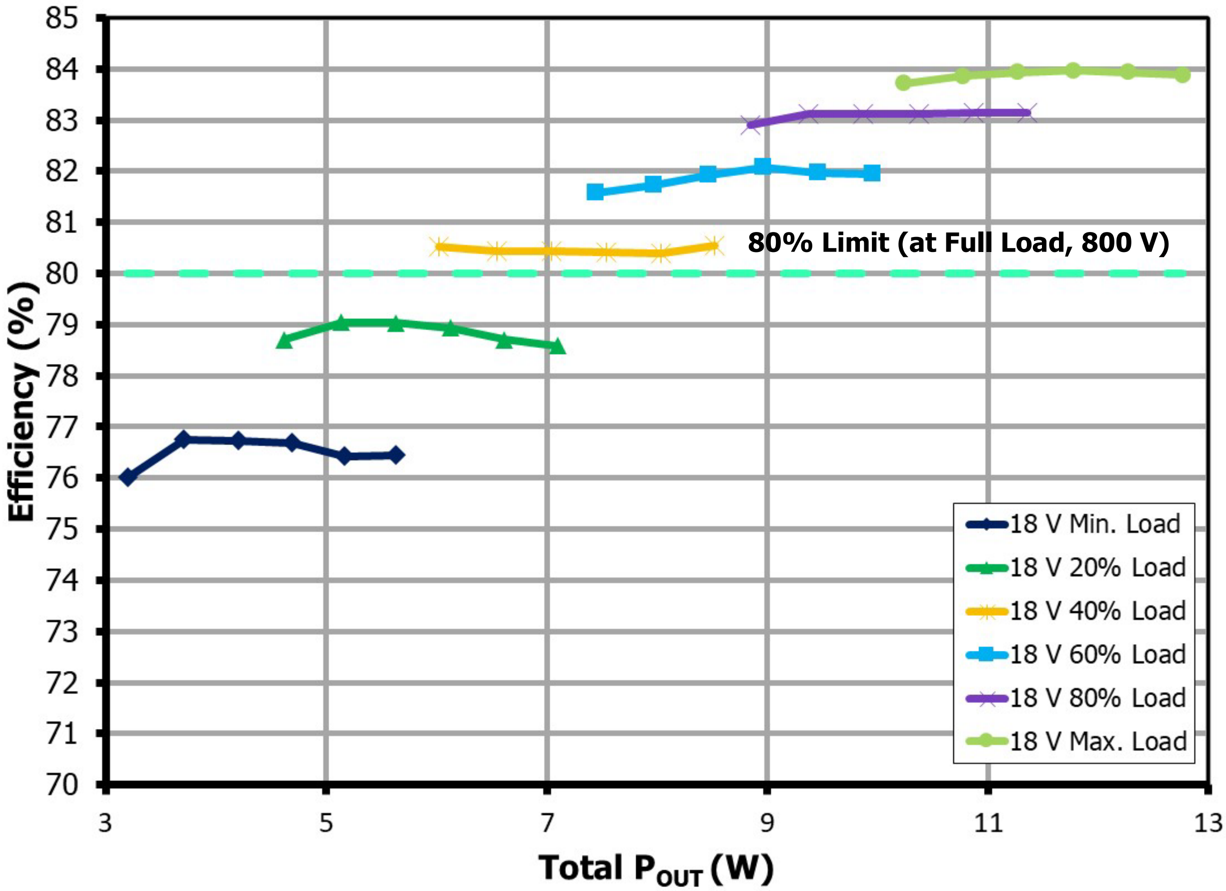


Figure 26 – Efficiency vs. Total Output Power at 800 V_{DC} Input and -40 °C Ambient Temperature.

9.2.2.4 1000 V_{DC} Input

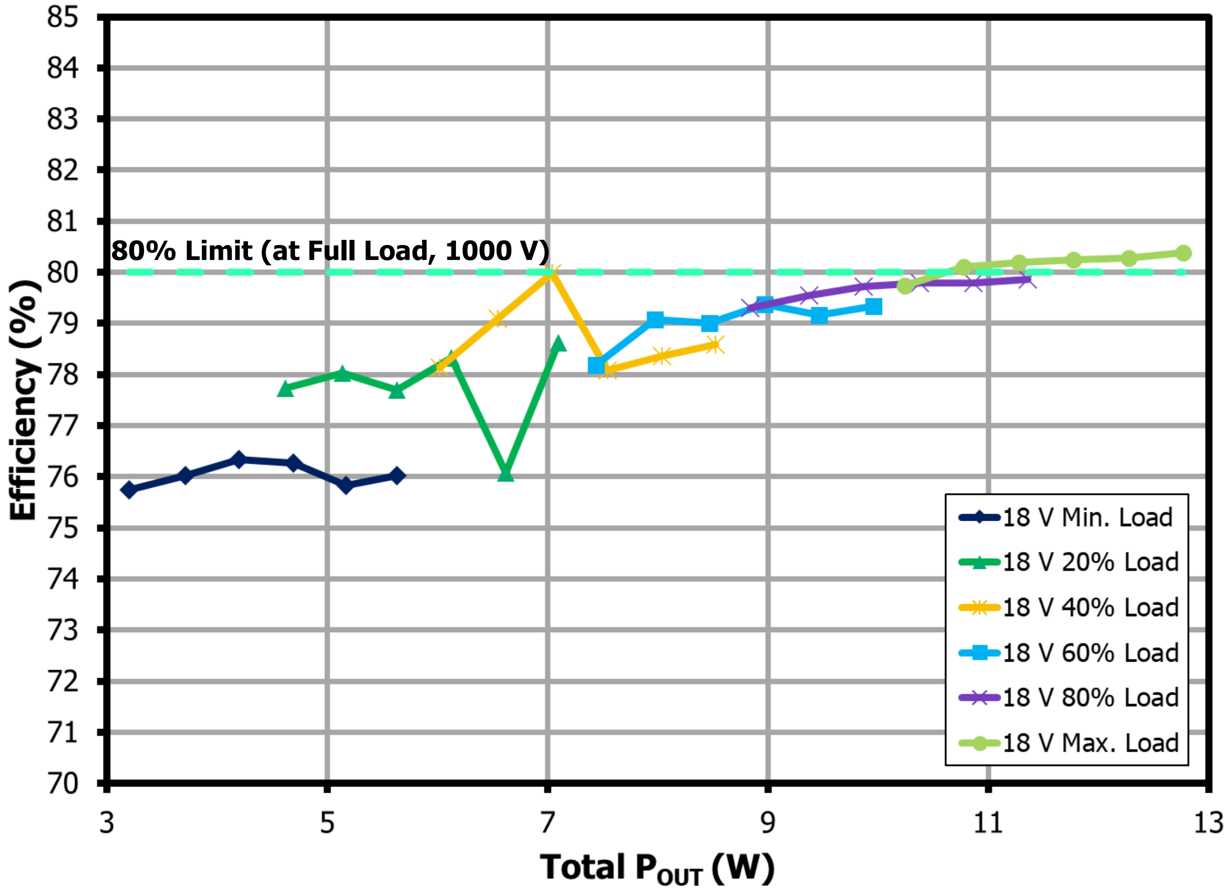


Figure 27 – Efficiency vs. Total Output Power at 1000 V_{DC} Input and 105 °C Ambient Temperature.

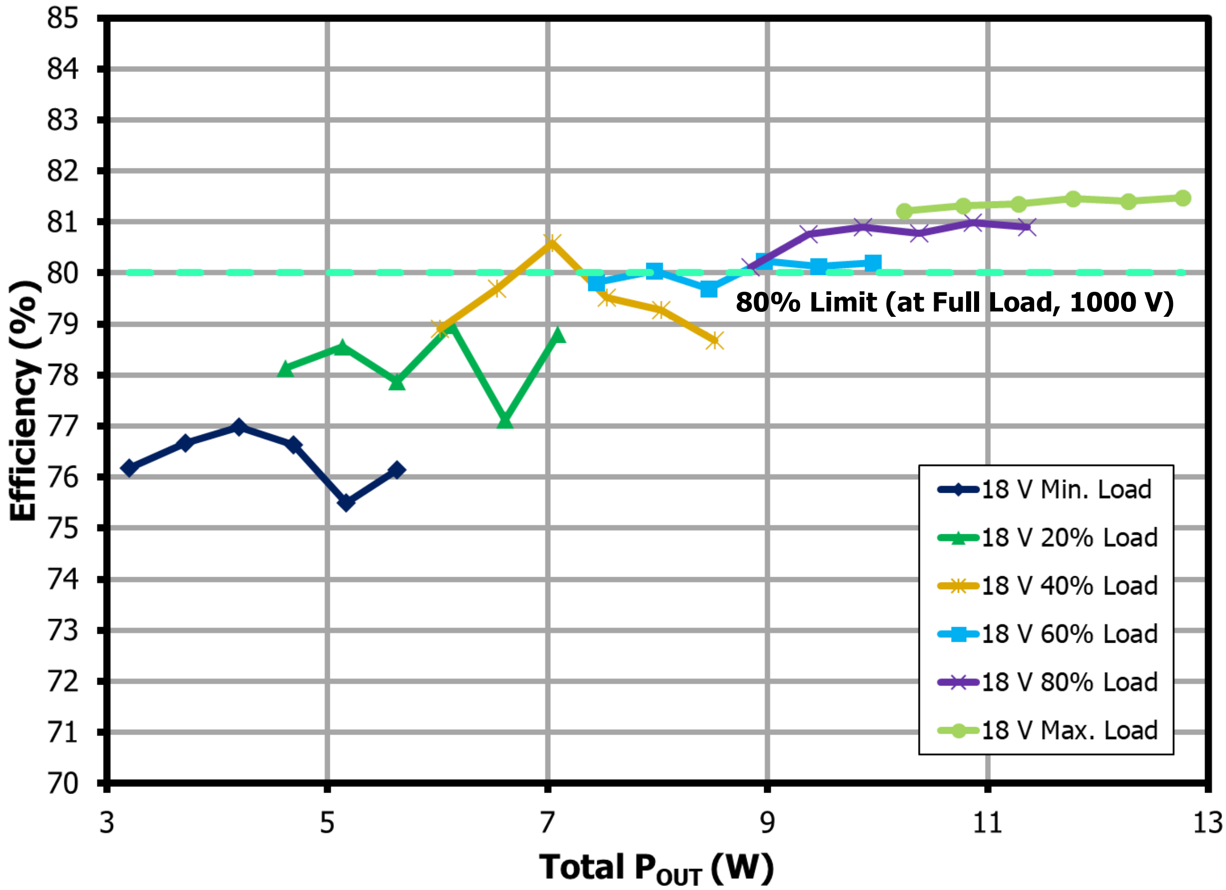


Figure 28 – Efficiency vs. Total Output Power at 1000 V_{DC} Input and 25 °C Ambient Temperature.

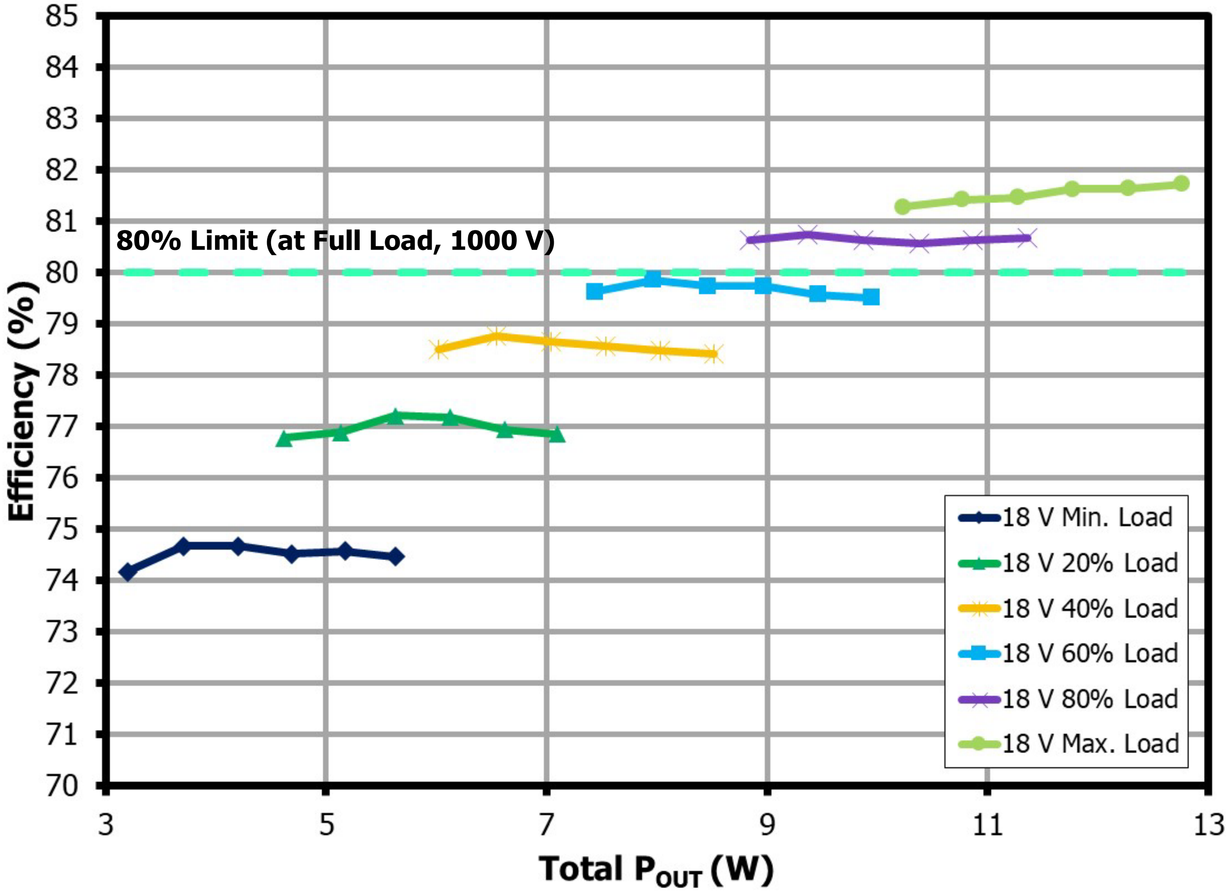


Figure 29 – Efficiency vs. Total Output Power at 1000 V_{DC} Input and -40 °C Ambient Temperature.

9.3 *Load Regulation*

Load regulation describes how loading conditions (minimum – maximum) affect the output voltage of the unit.

9.3.1 30 V_{DC} Input

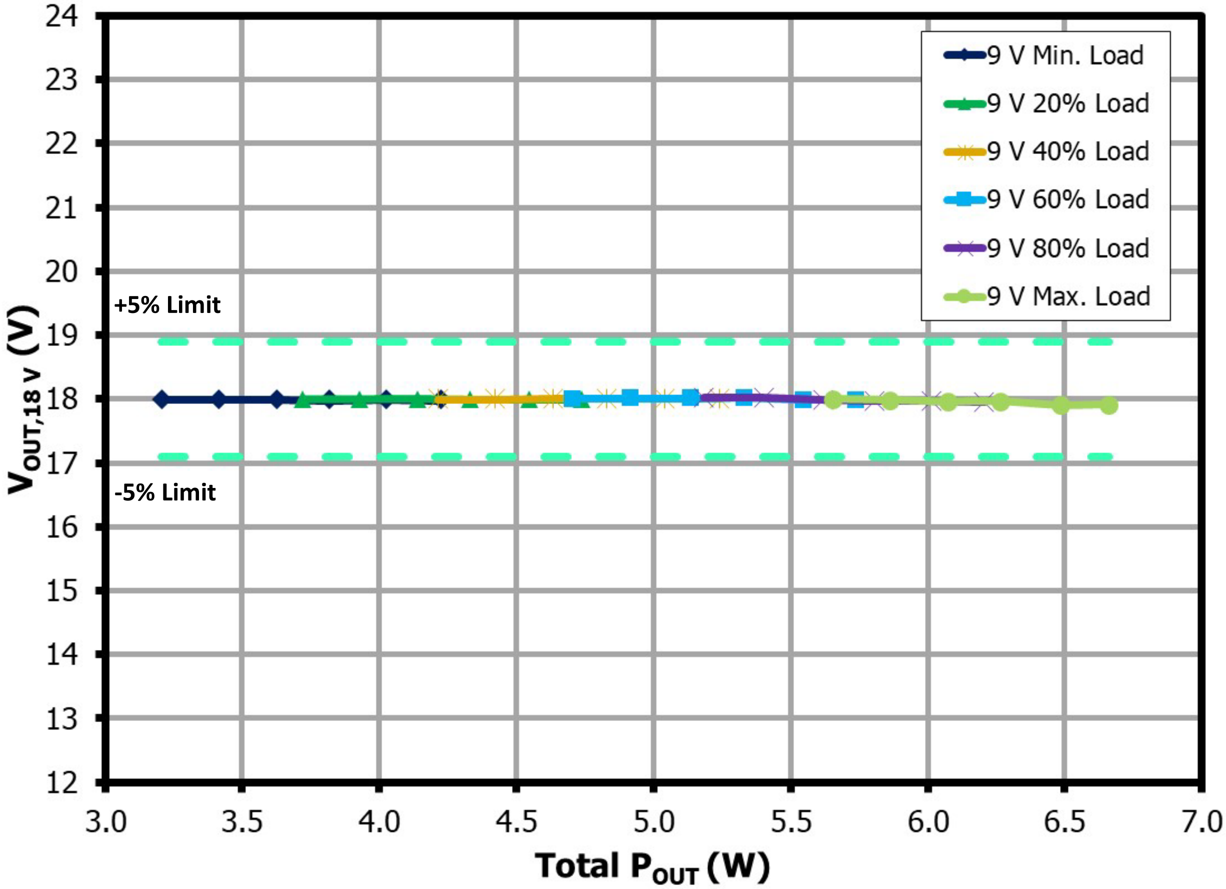


Figure 30 – 18 V Output Voltage vs. Total Output Power at 30 V_{DC} Input and 105 °C Ambient Temperature.[6]

[6] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

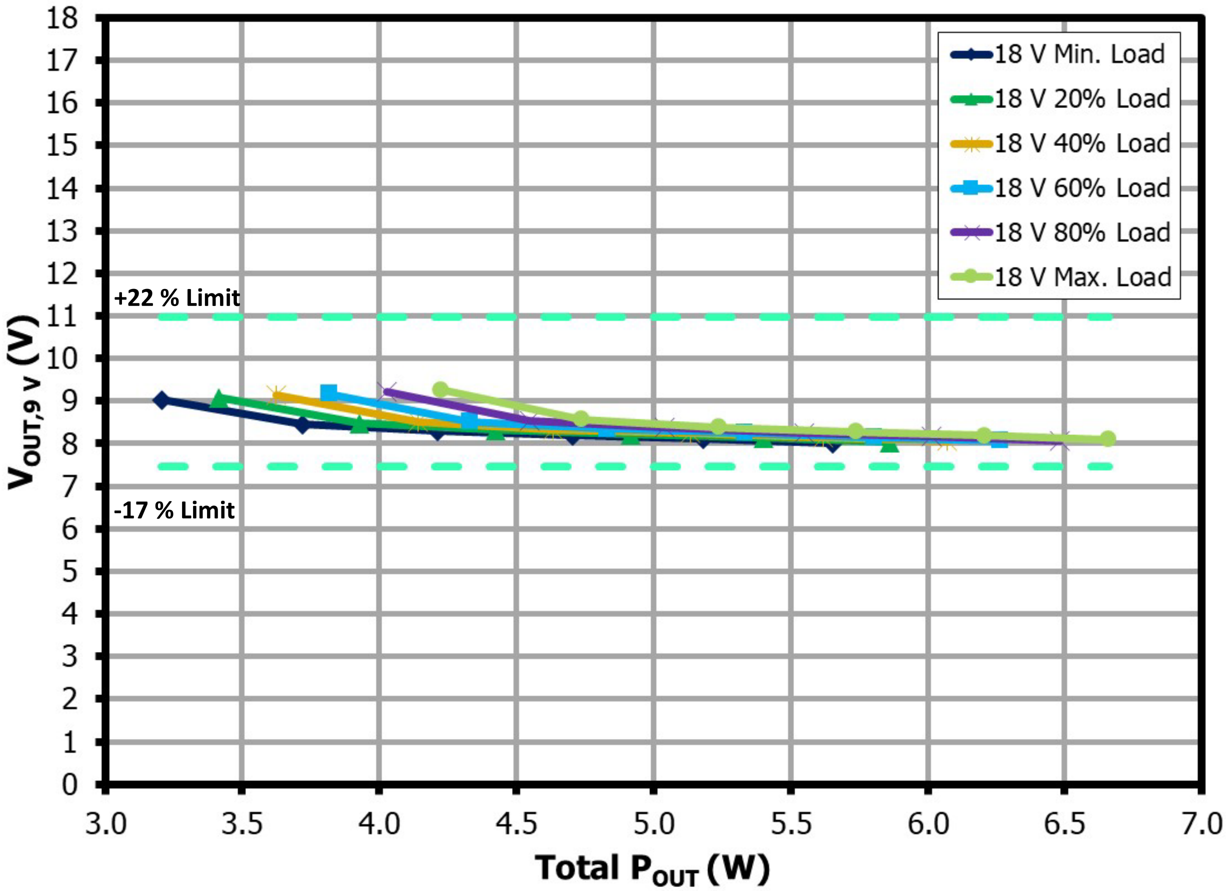


Figure 31 – 9 V Output Voltage vs. Total Output Power at 30 V_{DC} Input and 105 °C Ambient Temperature.[7]

[7] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

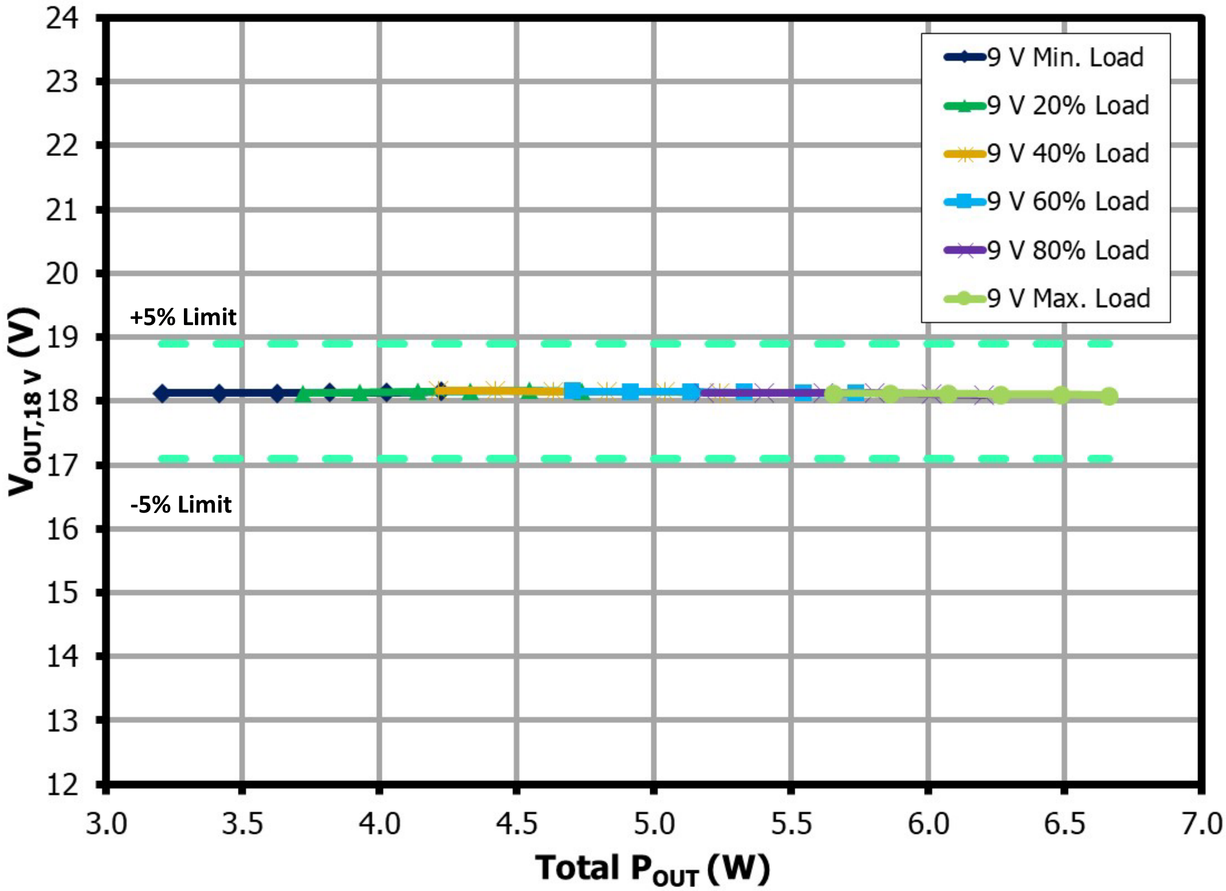


Figure 32 - 18 V Output Voltage vs. Total Output Power at 30 V_{DC} Input and -40 °C Ambient Temperature.[8]

[8] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

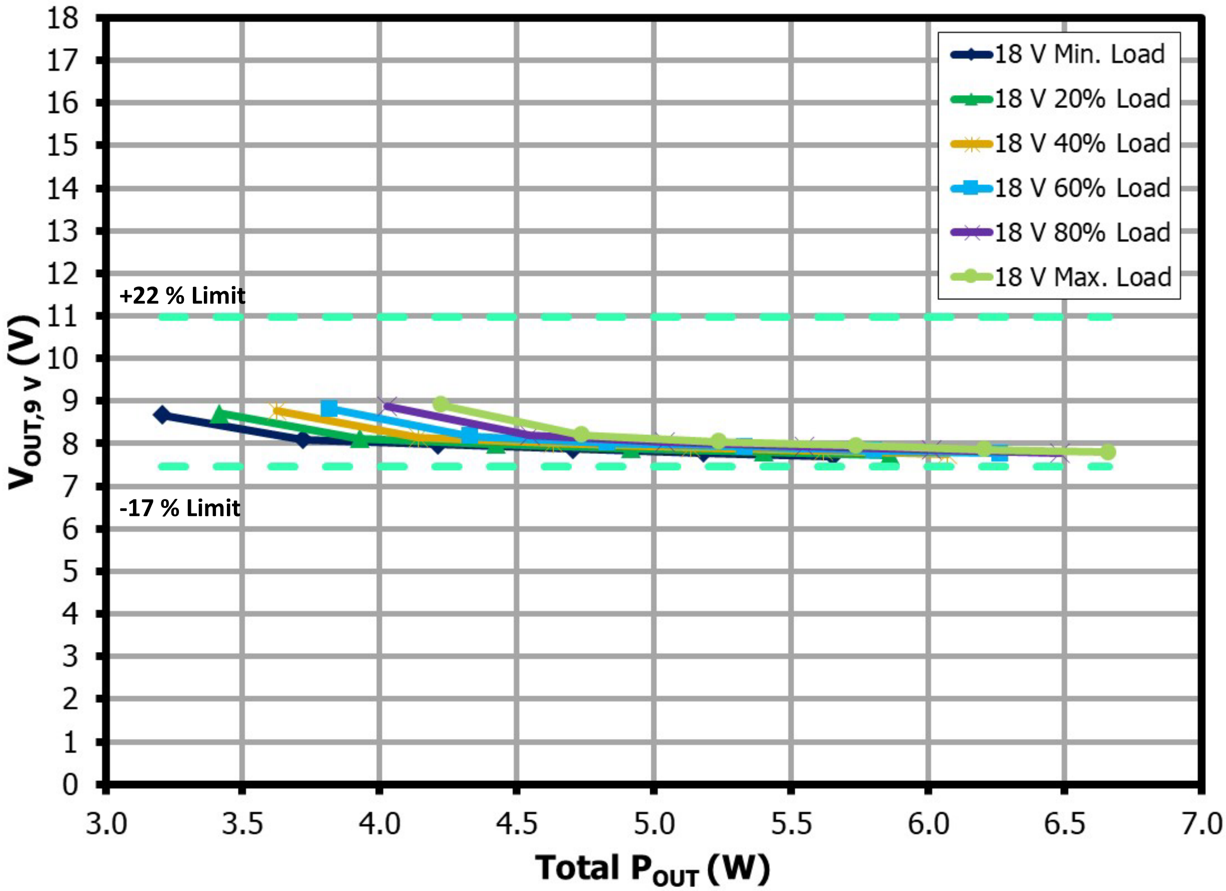


Figure 33 – 9 V Output Voltage vs. Total Output Power at 30 V_{DC} Input and -40 °C Ambient Temperature.[9]

[9] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

9.3.2 60 V_{DC} Input

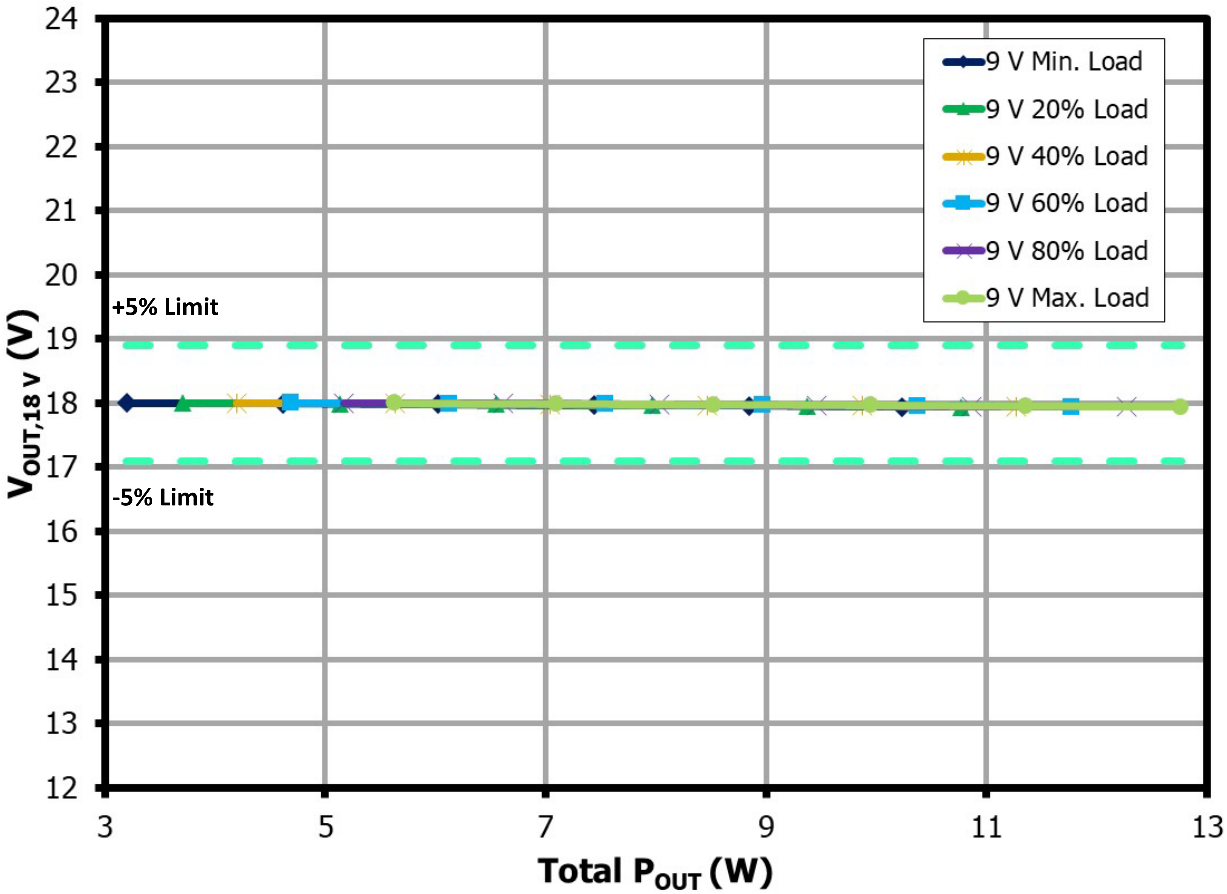


Figure 34 – 18 V Output Voltage vs. Total Output Power at 60 V_{DC} Input and 105 °C Ambient Temperature.[10]

[10] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

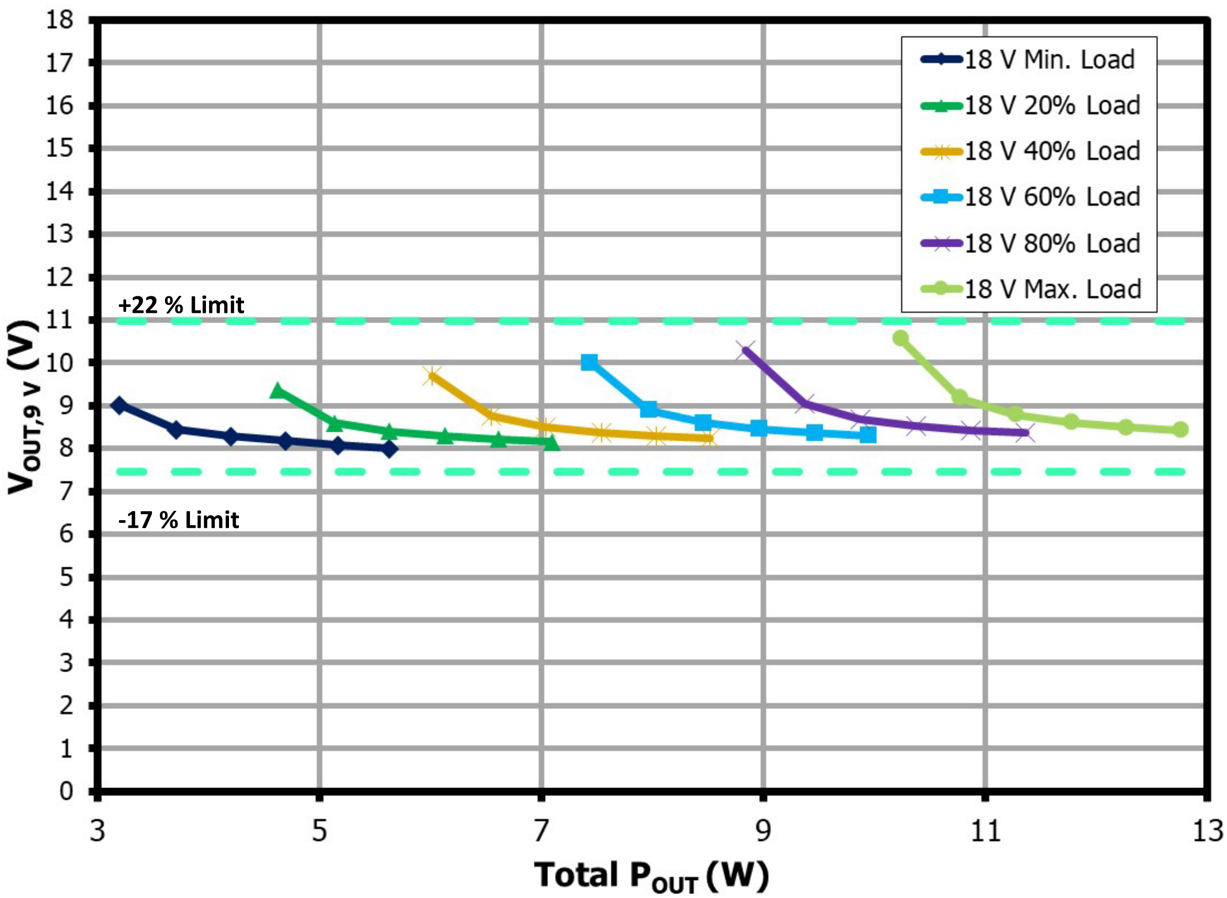


Figure 35 – 9 V Output Voltage vs. Total Output Power at 60 V_{DC} Input and 105 °C Ambient Temperature.[11]

[11] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

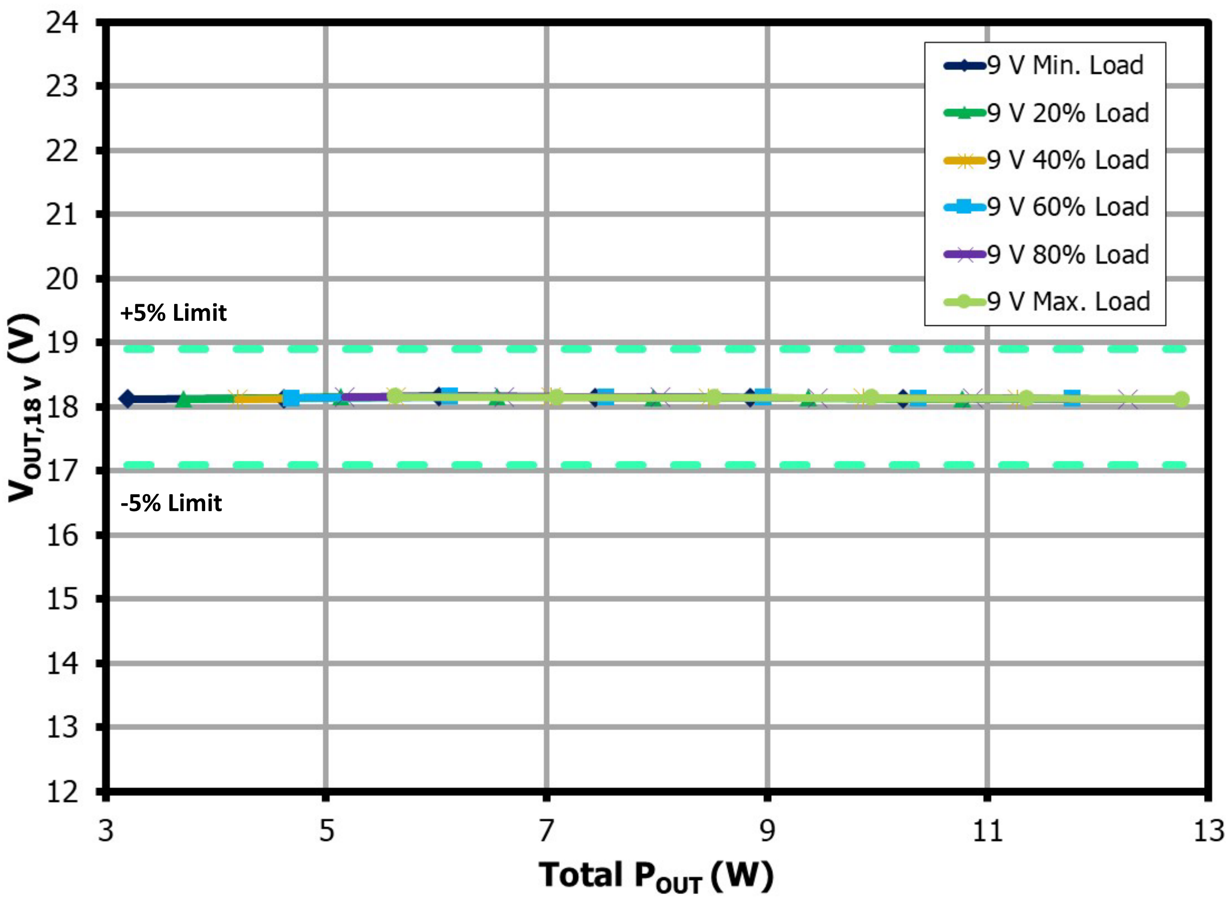


Figure 36 – 18 V Output Voltage vs. Total Output Power at 60 V_{DC} Input and -40 °C Ambient Temperature.[12]

[12] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

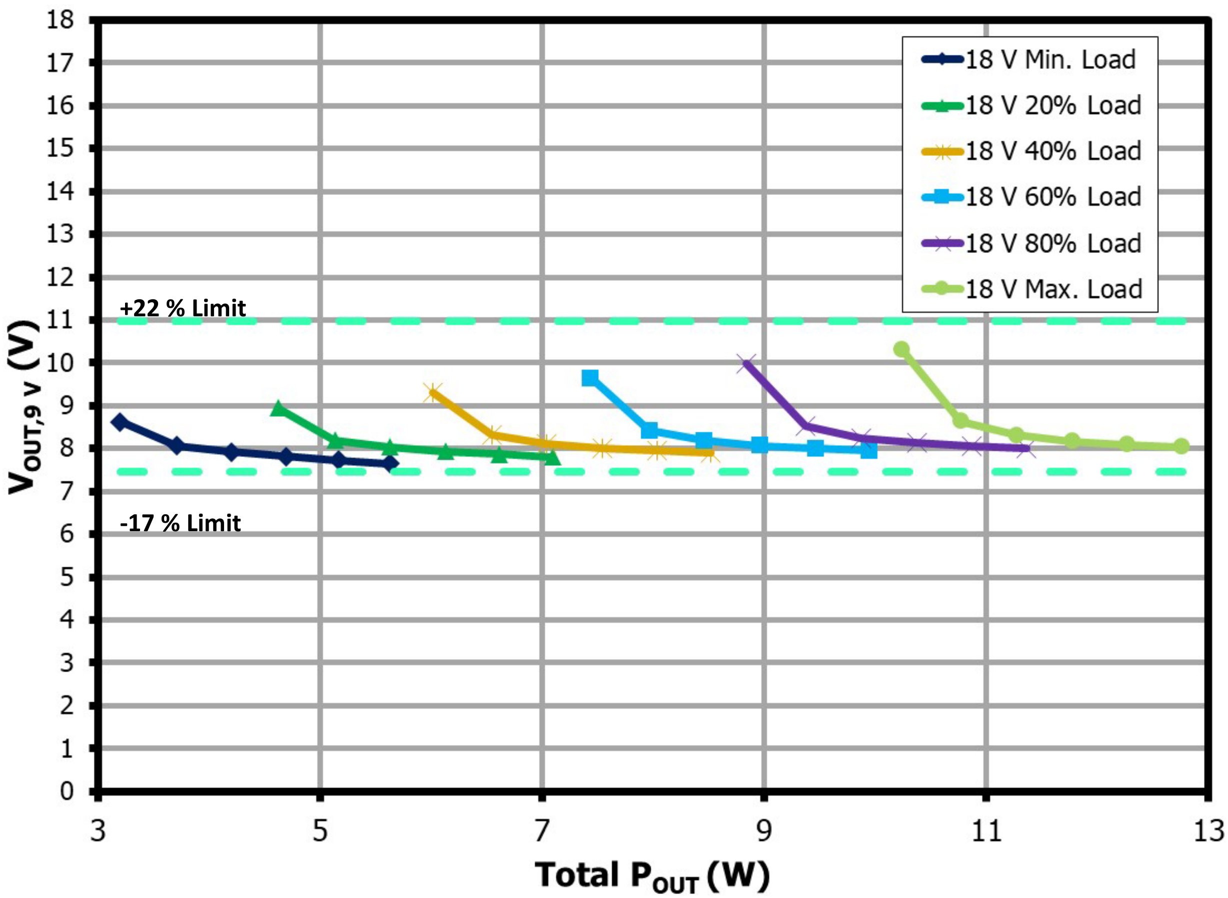


Figure 37 – 9 V Output Voltage vs. Total Output Power at 60 V_{DC} Input and -40 °C Ambient Temperature.[13]

[13] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

9.3.3 800 V_{DC} Input

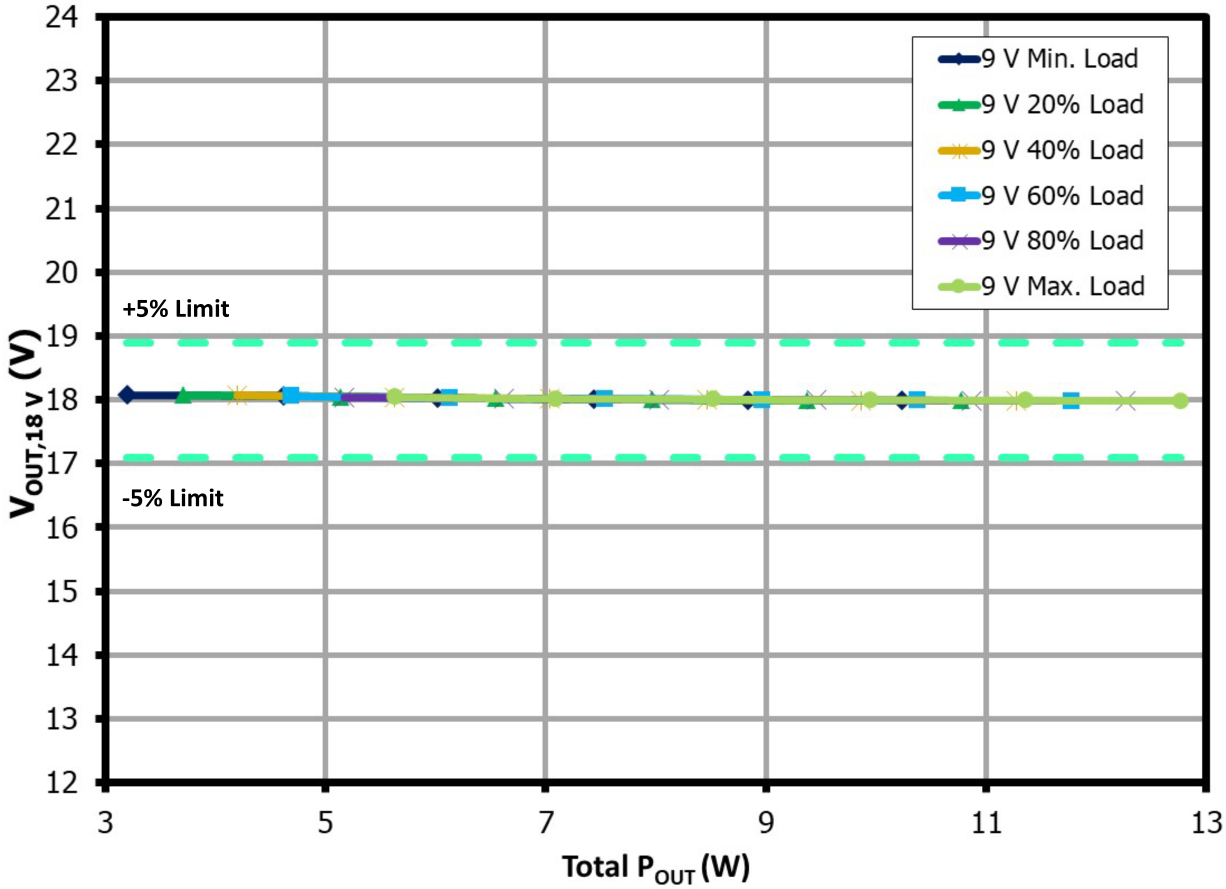


Figure 38 – 18 V Output Voltage vs. Total Output Power at 800 V_{DC} Input and 105 °C Ambient Temperature.[14]

[14] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

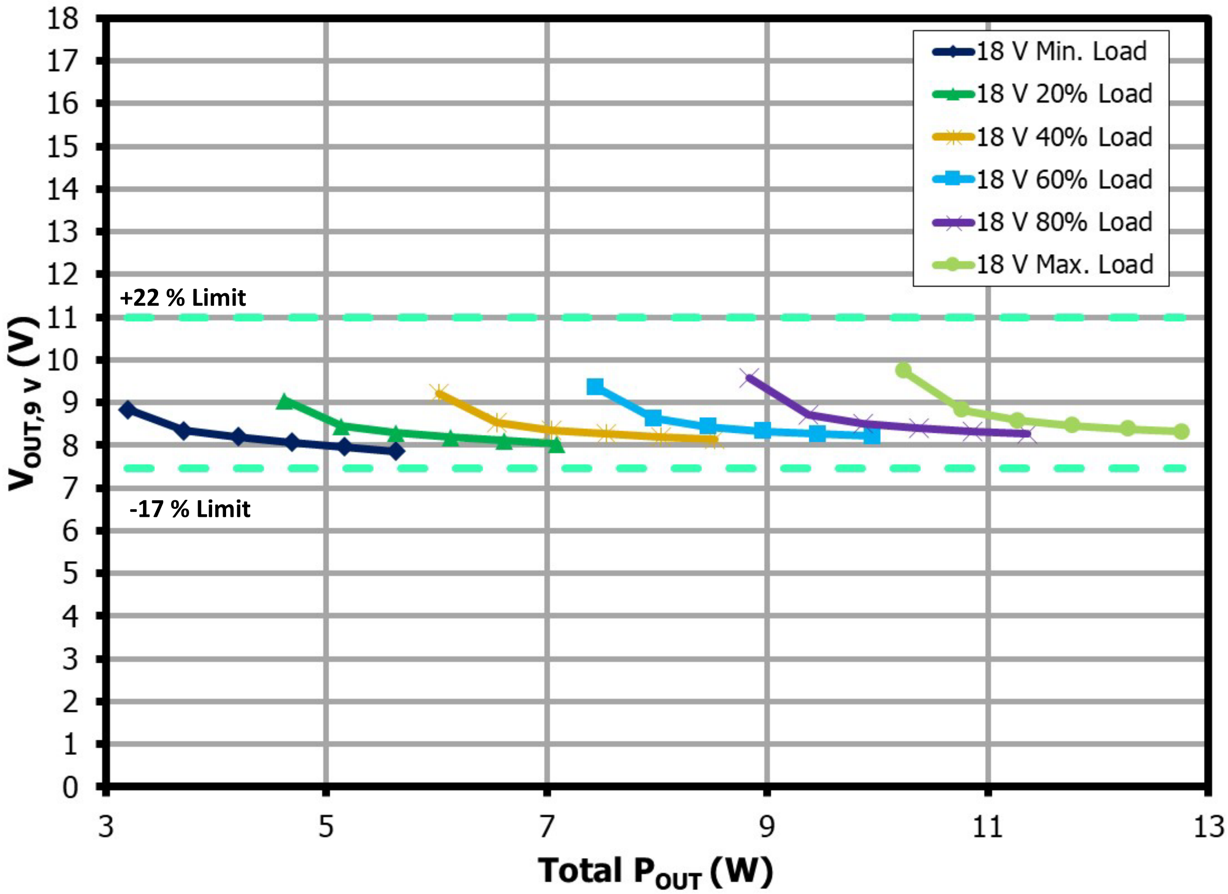


Figure 39 – 9 V Output Voltage vs. Total Output Power at 800 V_{DC} Input and 105 °C Ambient Temperature.[15]

[15] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

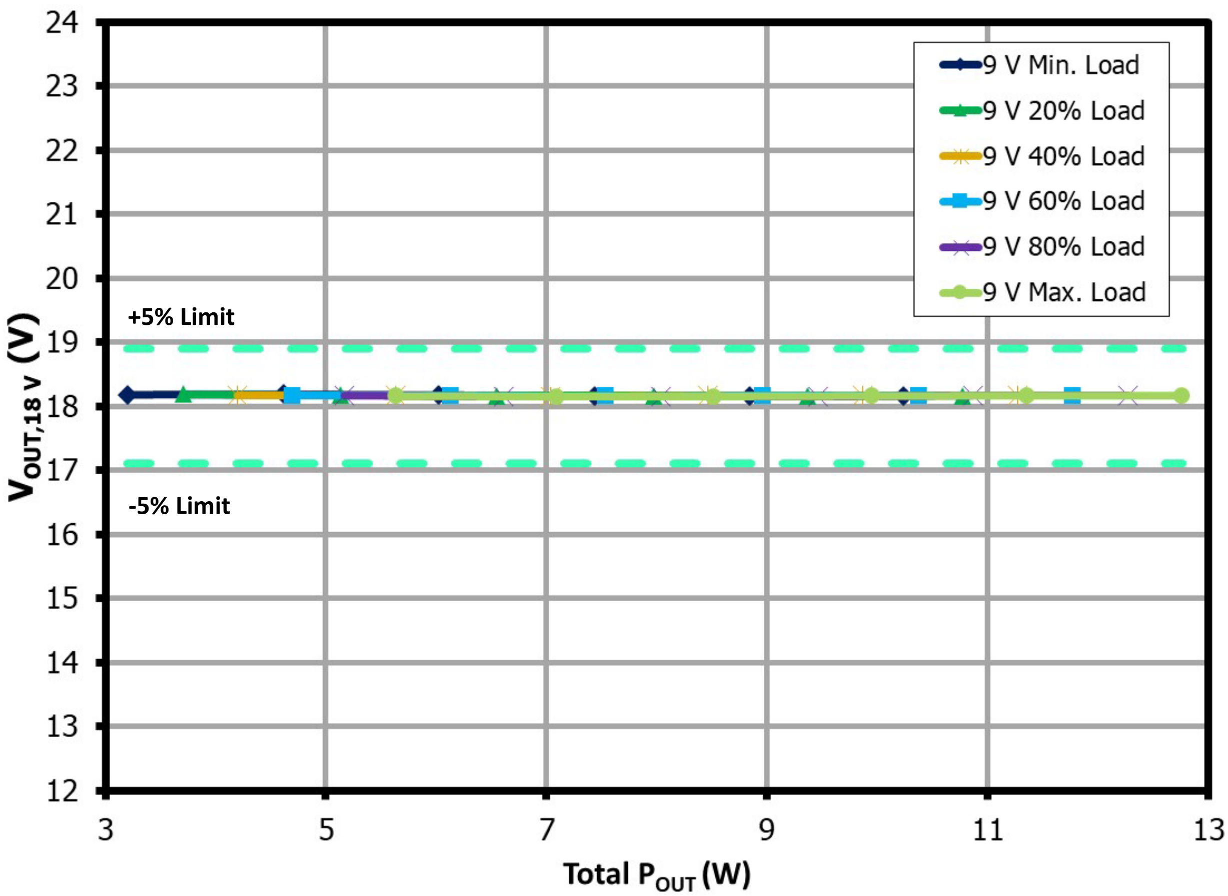


Figure 40 – 18 V Output Voltage vs. Total Output Power at 800 V_{DC} Input and -40 °C Ambient Temperature.[16]

[16] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

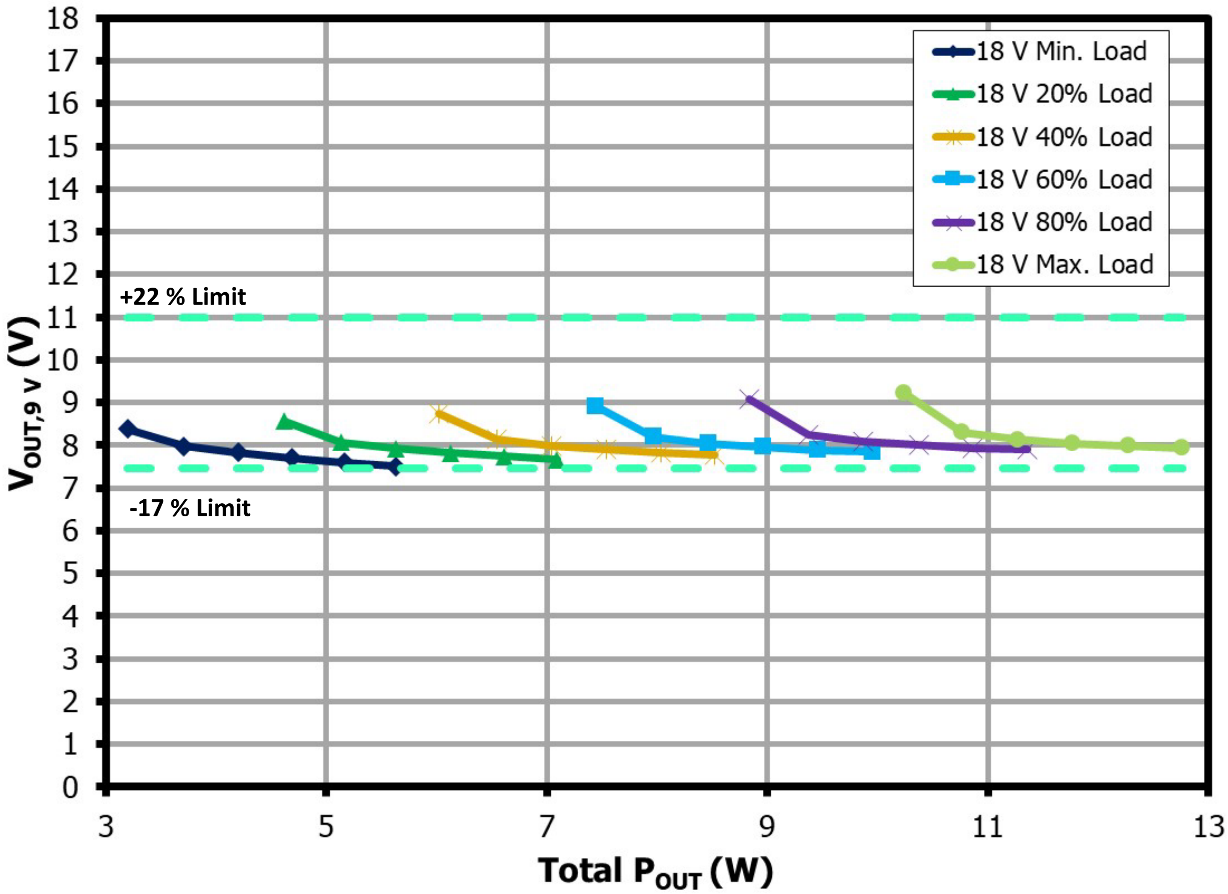


Figure 41 – 9 V Output Voltage vs. Total Output Power at 800 V_{DC} Input and -40 °C Ambient Temperature.[17]

[17] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

9.3.4 1000 V_{DC} Input

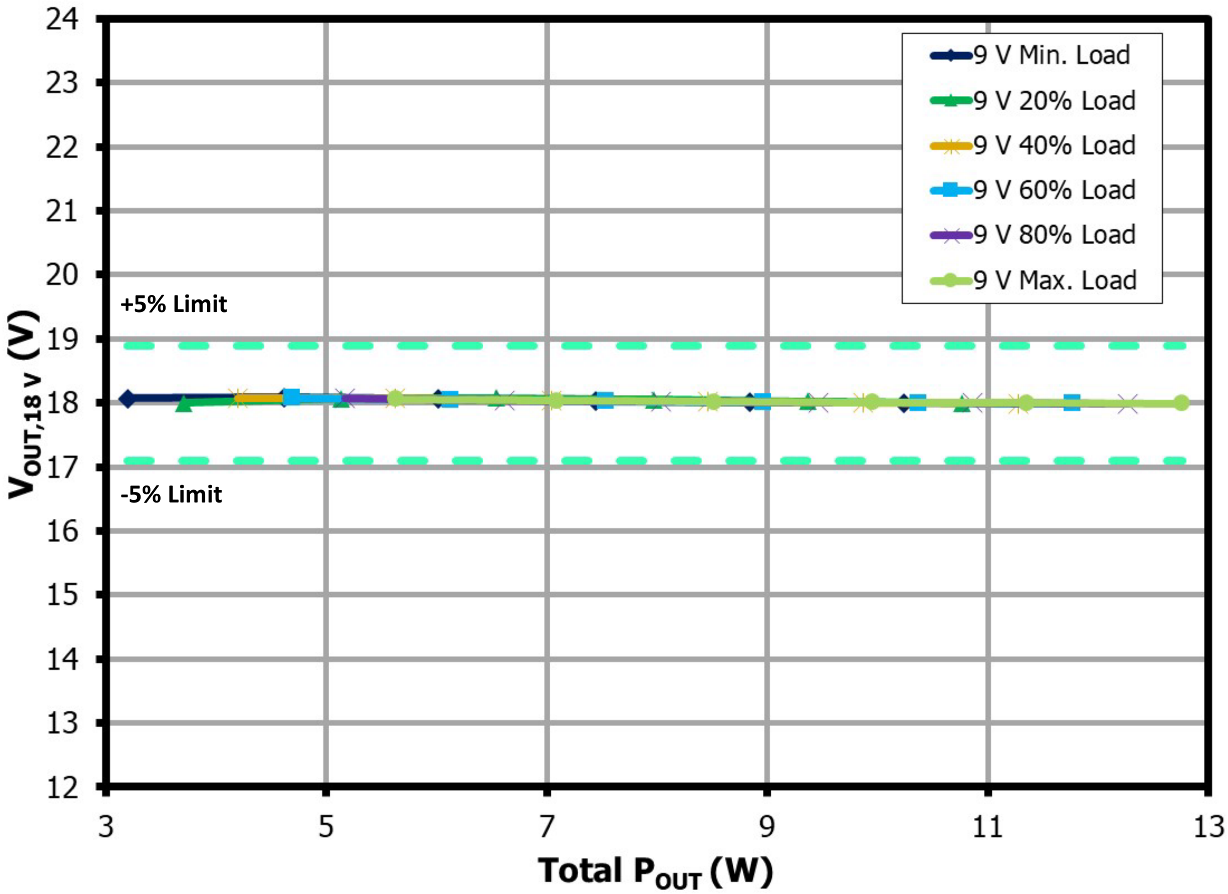


Figure 42 – 18 V Output Voltage vs. Total Output Power at 1000 V_{DC} Input and 105 °C Ambient Temperature.[18]

[18] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

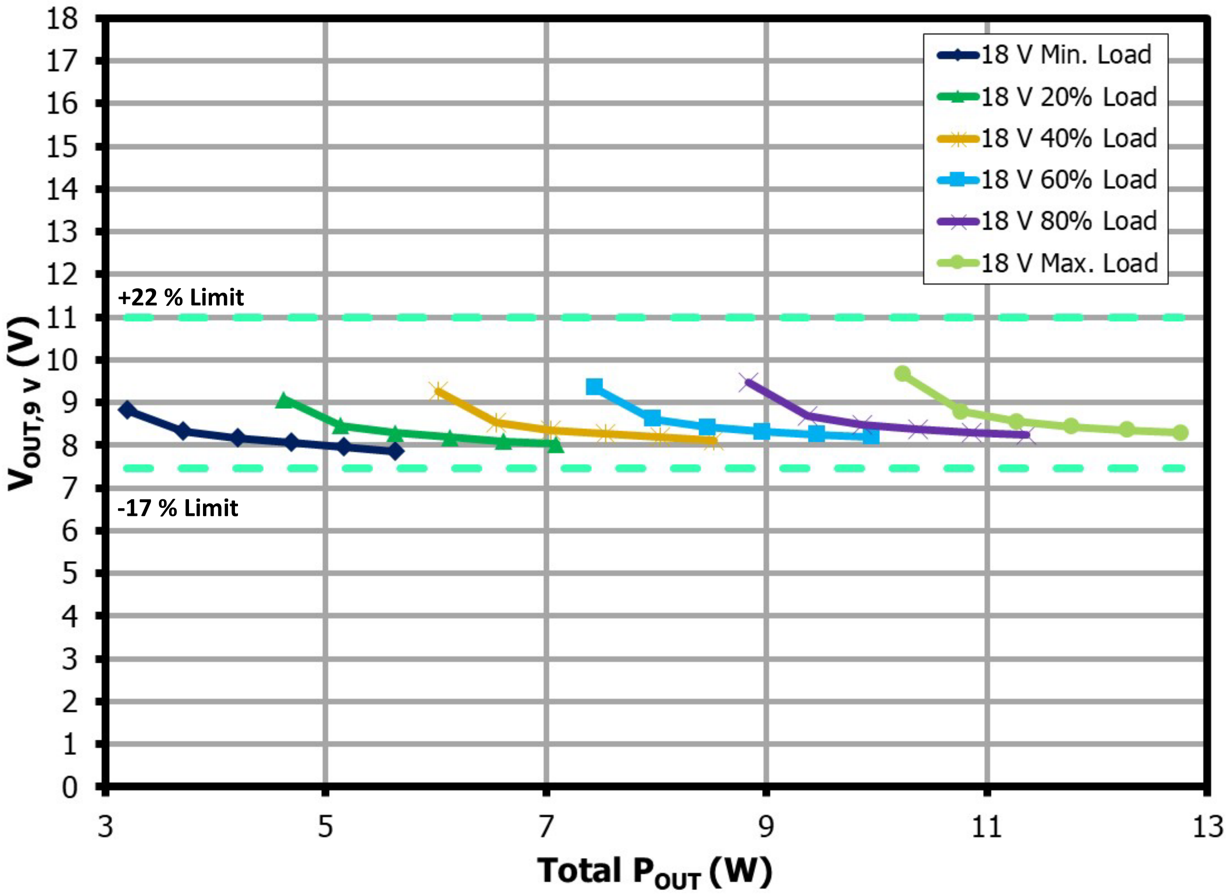


Figure 43 – 9 V Output Voltage vs. Total Output Power at 1000 V_{DC} Input and 105 °C Ambient Temperature.[19]

[19] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

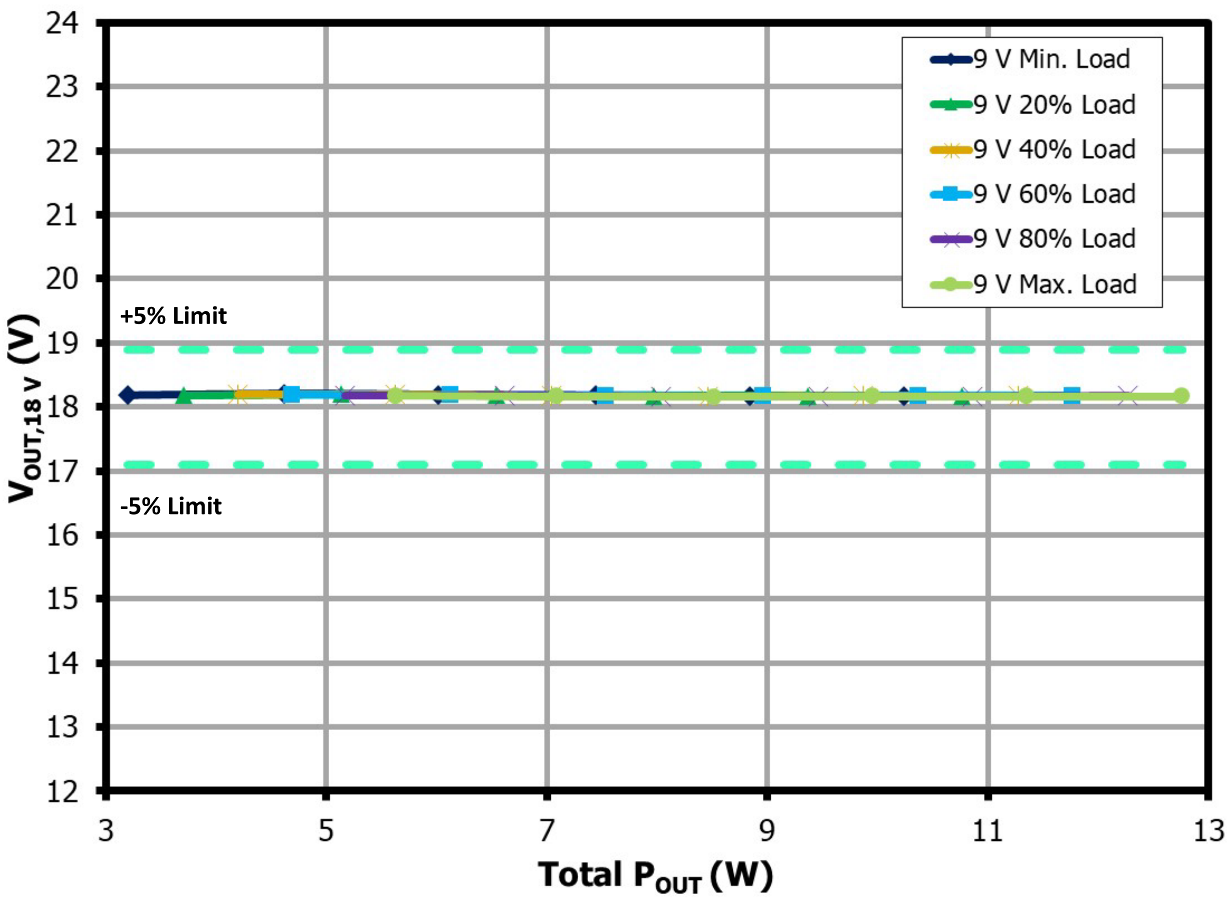


Figure 44 – 18 V Output Voltage vs. Total Output Power at 1000 V_{DC} Input and -40 °C Ambient Temperature.[20]

[20] Each line represents the 18 V output regulation vs. total output power of the unit under test when the 9 V output load is maintained at a certain percentage while the 18 V output load is increased from its minimum to maximum loading condition.

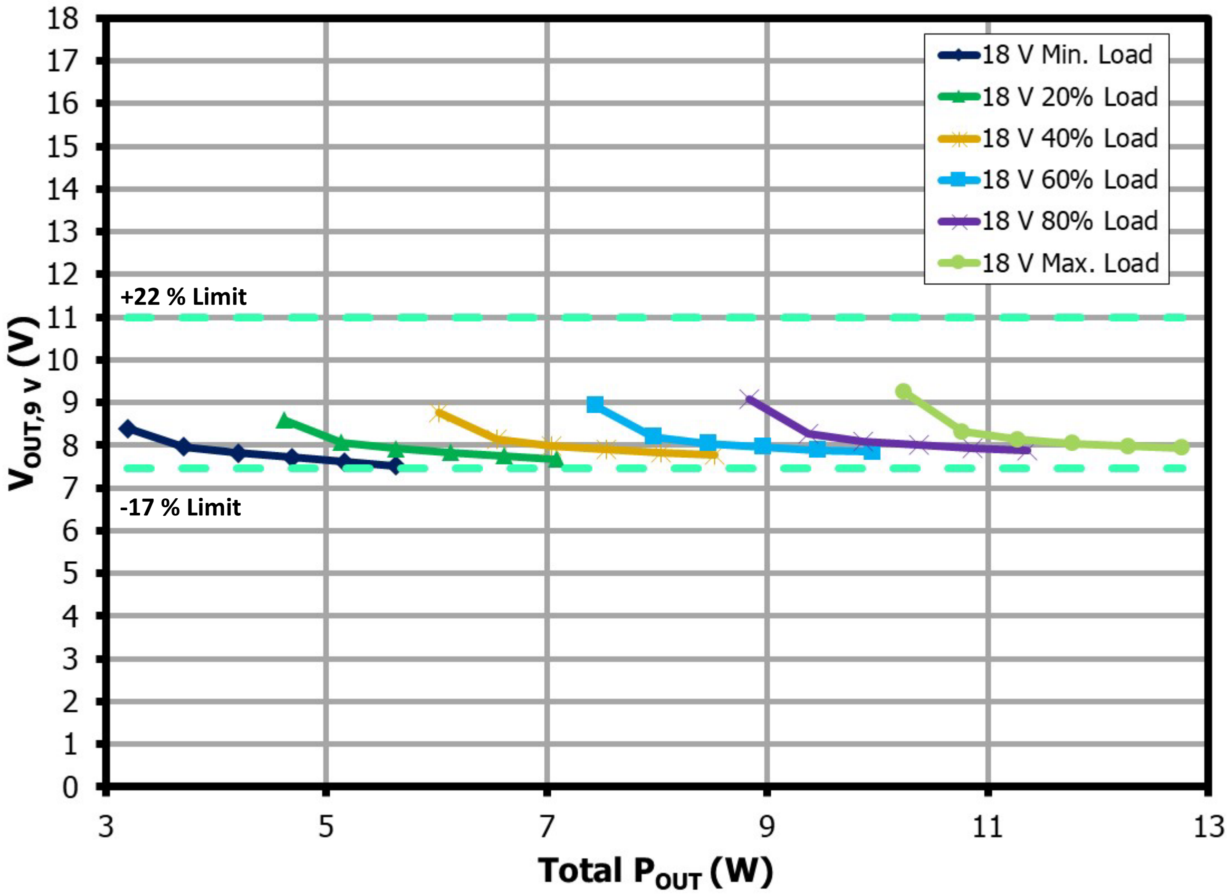


Figure 45 – 9 V Output Voltage vs. Total Output Power at 1000 V_{DC} Input and -40 °C Ambient Temperature.[21]

[21] Each line represents the 9 V output regulation vs. total output power of the unit under test when the 18 V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

9.4 *Line Regulation*

Line regulation describes how the change in input voltage affects the output voltage of the unit.

9.4.1 Loading Condition: 18 V = Max. / 9 V = Max.

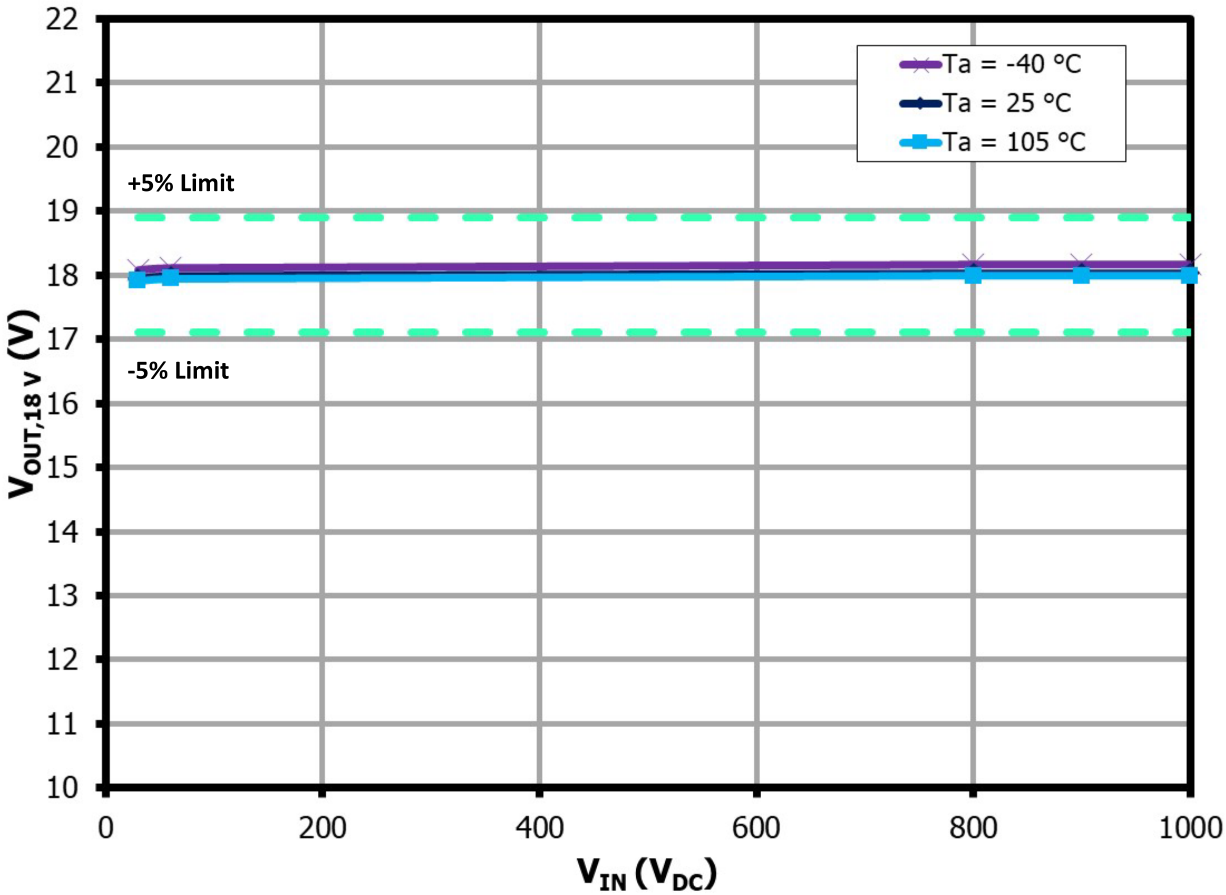


Figure 46 – 18 V Output Voltage vs. Input Line Voltage.

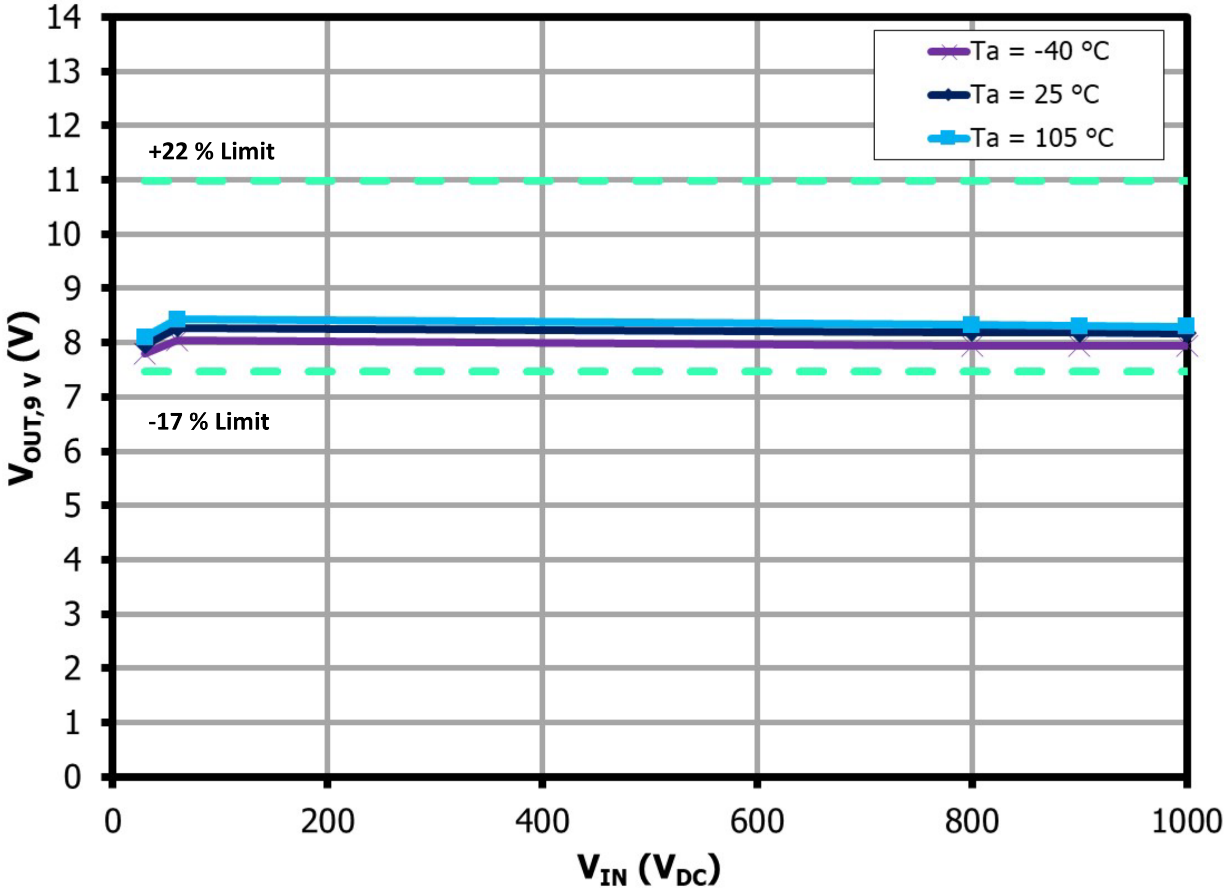


Figure 47 – 9 V Output Voltage vs. Input Line Voltage.

9.4.2 Loading Condition: 18 V = Max. / 9 V = Min.

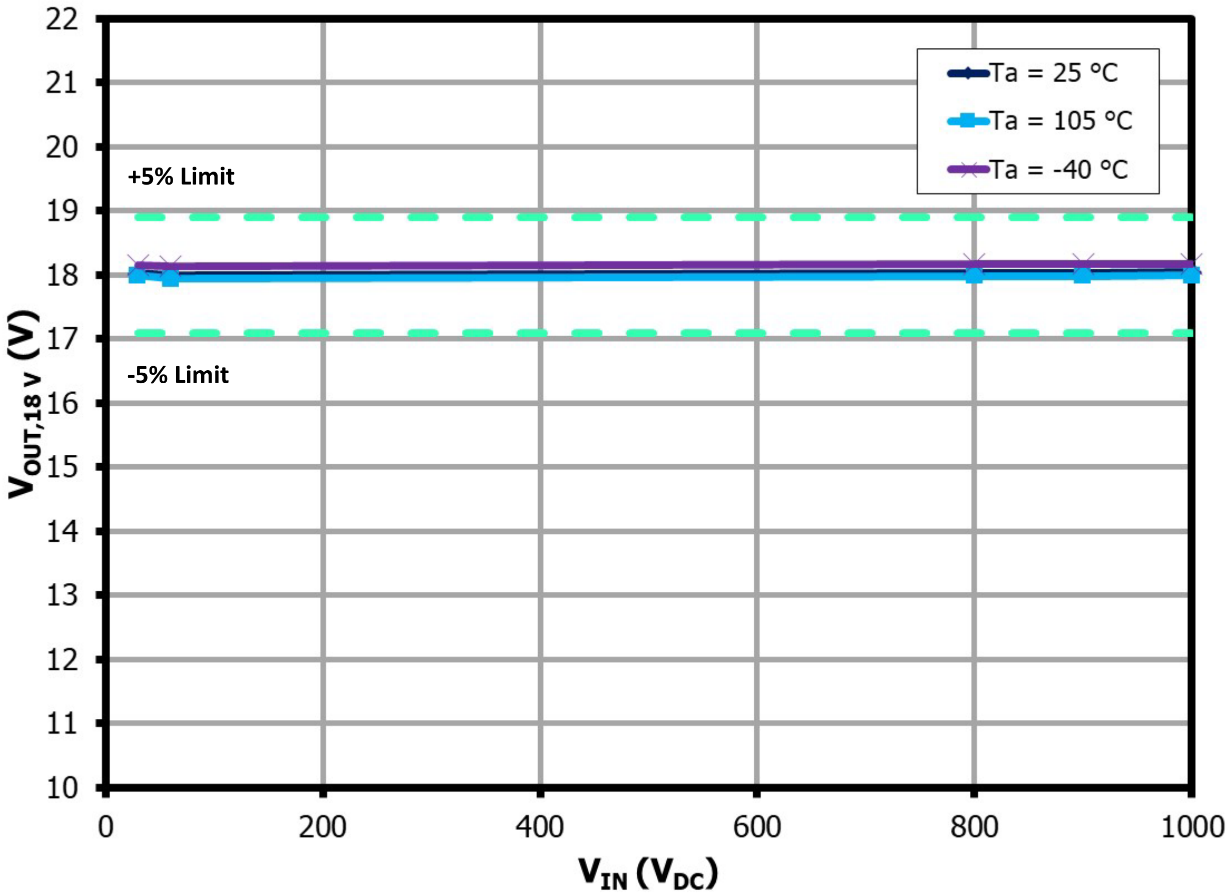


Figure 48 – 18 V Output Voltage vs. Input Line Voltage.

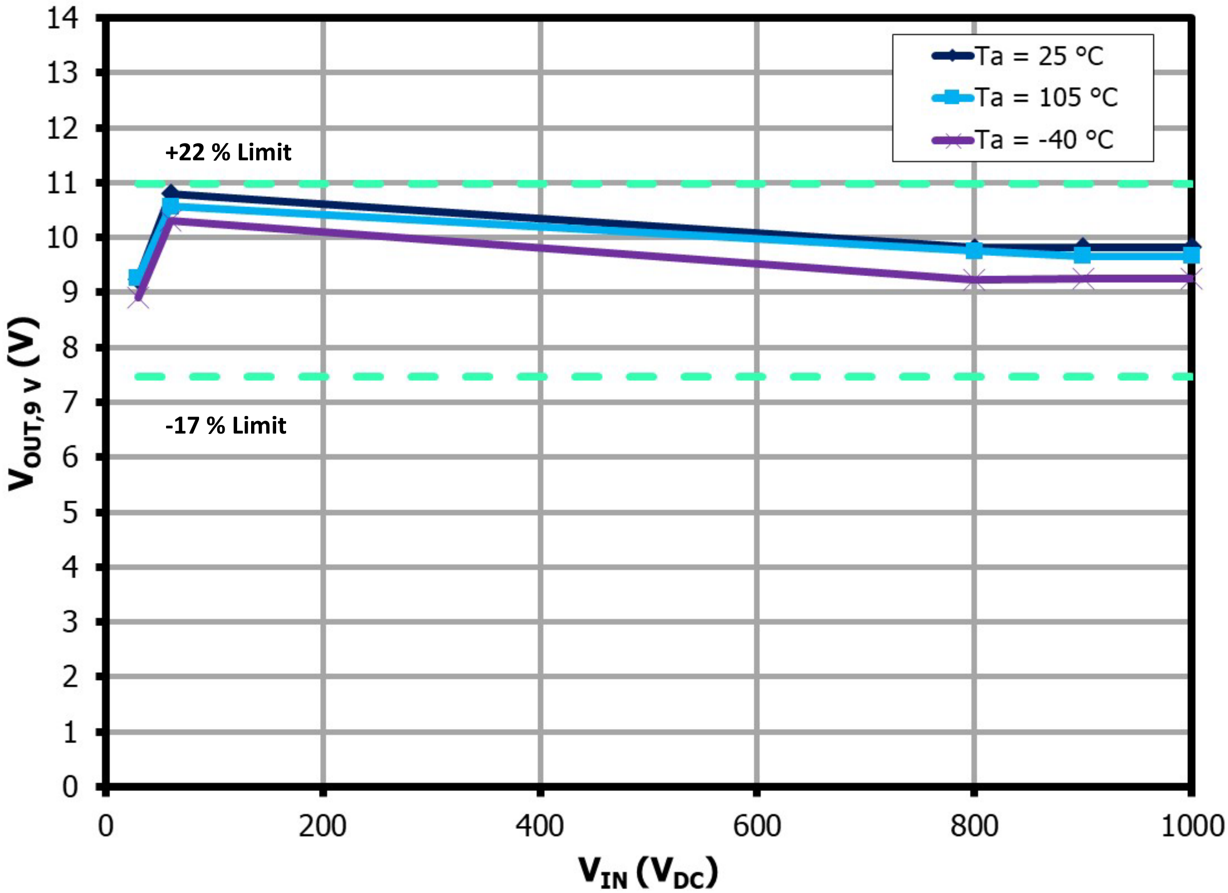


Figure 49 – 9 V Output Voltage vs. Input Line Voltage.

9.4.3 Loading Condition: 18 V = Min. / 9 V = Max.

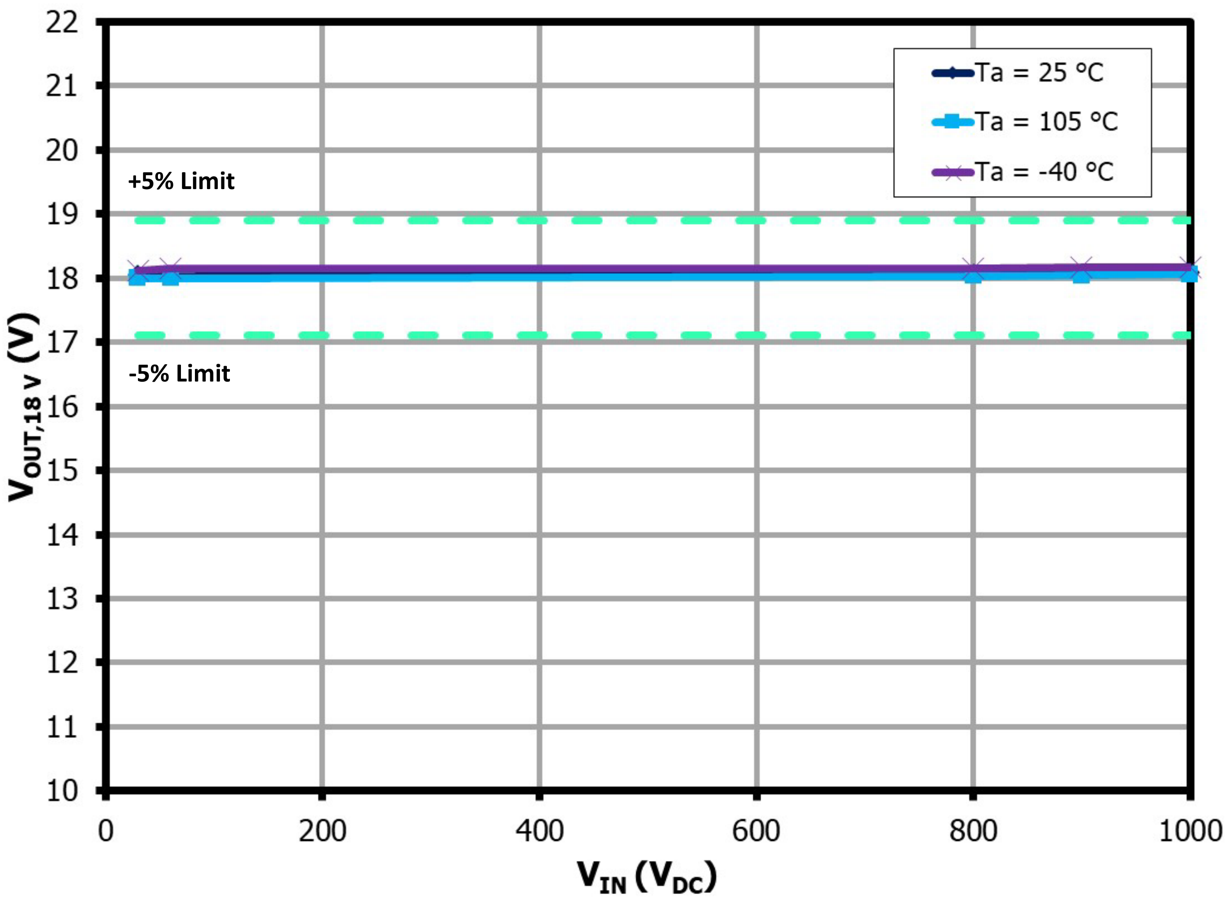


Figure 50 – 18 V Output Voltage vs. Input Line Voltage.

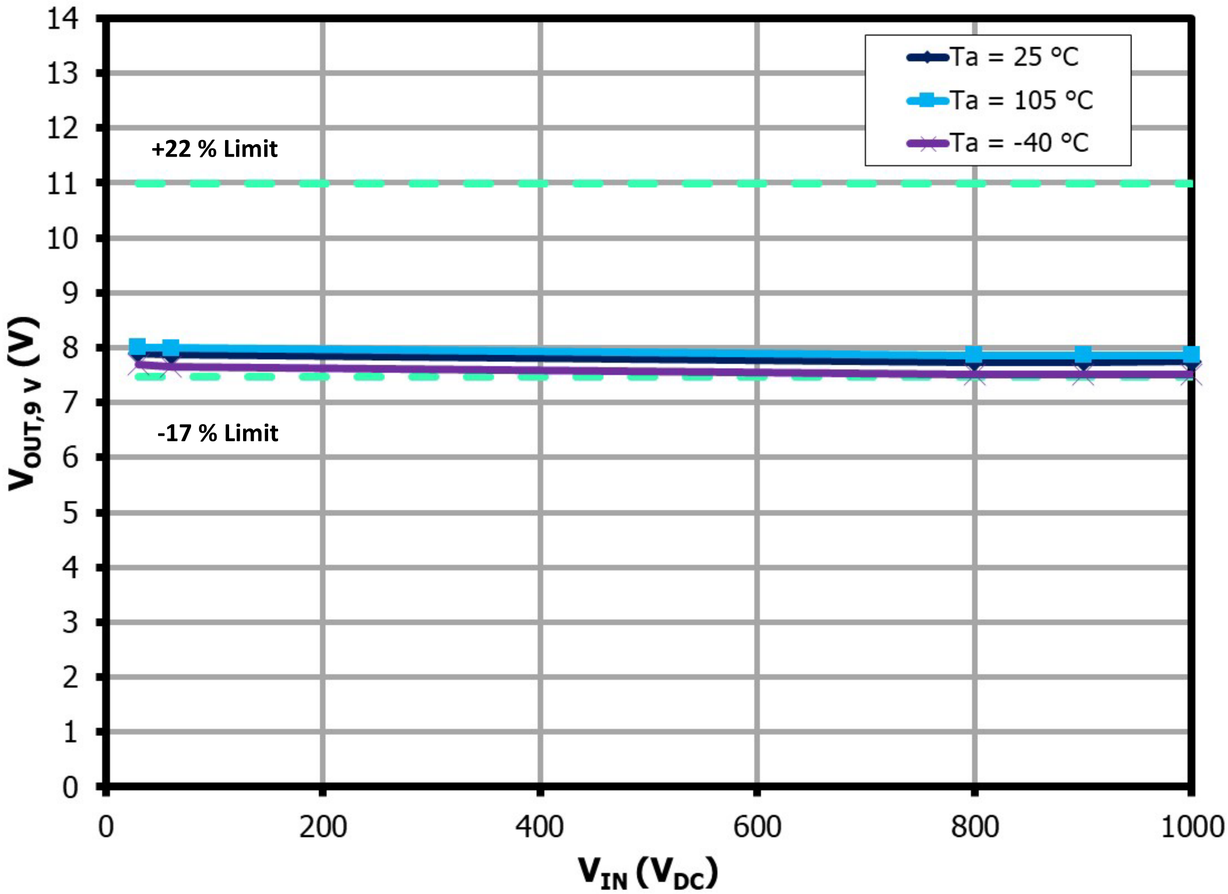


Figure 51 – 9 V Output Voltage vs. Input Line Voltage.

10 Thermal Performance

10.1 *Thermal Data at 105 °C Ambient Temperature*

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 105 °C for at least 30 minutes before turning on the unit under test. The following measurements were taken after soaking the unit for at least one (1) hour to allow component temperatures to stabilize.

Critical Components	Input Voltage			
	30 V	60 V	800 V	1000 V
Input CMC	118.8 °C	124.1 °C	126.4 °C	127.5 °C
Transformer Pri-Sec Wire	119.4 °C	124.4 °C	127.7 °C	128.1 °C
Transformer Sec-Pri Wire	119.2 °C	124.0 °C	127.3 °C	127.8 °C
Transformer Pri-air Wire	117.9 °C	122.4 °C	124.8 °C	125.6 °C
Transformer Core	116.4 °C	120.6 °C	124.2 °C	124.8 °C
18 V SR FET	116.1 °C	119.8 °C	120.5 °C	121.8 °C
Secondary Snubber Resistor	115.5 °C	118.8 °C	121.7 °C	122.1 °C
18 V Cout	113.9 °C	116.9 °C	117.1 °C	118.1 °C
18 V Lfilter	114.3 °C	120.4 °C	118.5 °C	120.8 °C
18 V Cfilter	113.4 °C	116.1 °C	115.5 °C	116.4 °C
9 V Freewheeling diode	123.7 °C	125.2 °C	125.3 °C	125.5 °C
Primary Snubber Resistor	118.3 °C	121.1 °C	120.0 °C	120.6 °C
INN3949CQ	121.4 °C	124.6 °C	129.1 °C[22]	131.1 °C
Ambient Temperature	104.9 °C	105.9 °C	103.6 °C	103.5 °C

Table 8 – Summary of DER-956Q Critical Components at 105 °C Operating Temperature.

[22] Increasing the cooling area in the actual design or having a provision for heat sink or thermal pad between source area of the device and the enclosure is recommended.

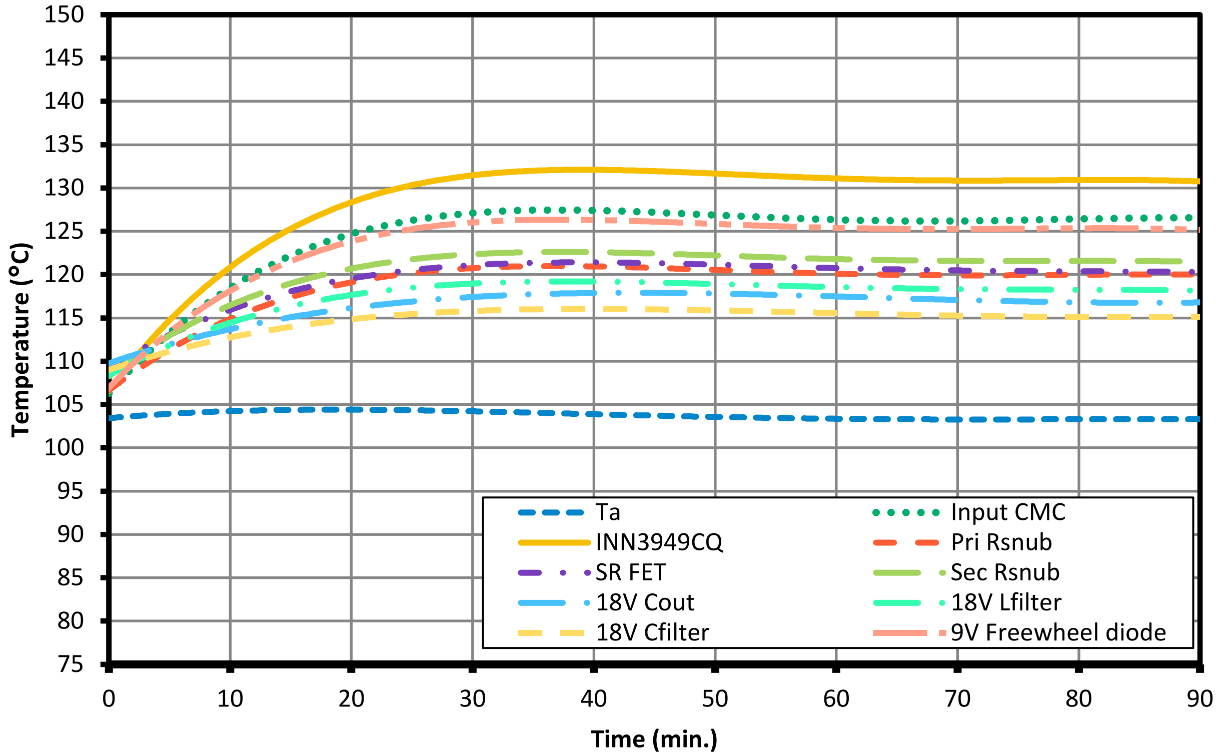


Figure 52 – 1000 V_{DC} Input, 13 W Output Operating Temperature of DER-956Q Critical Components.

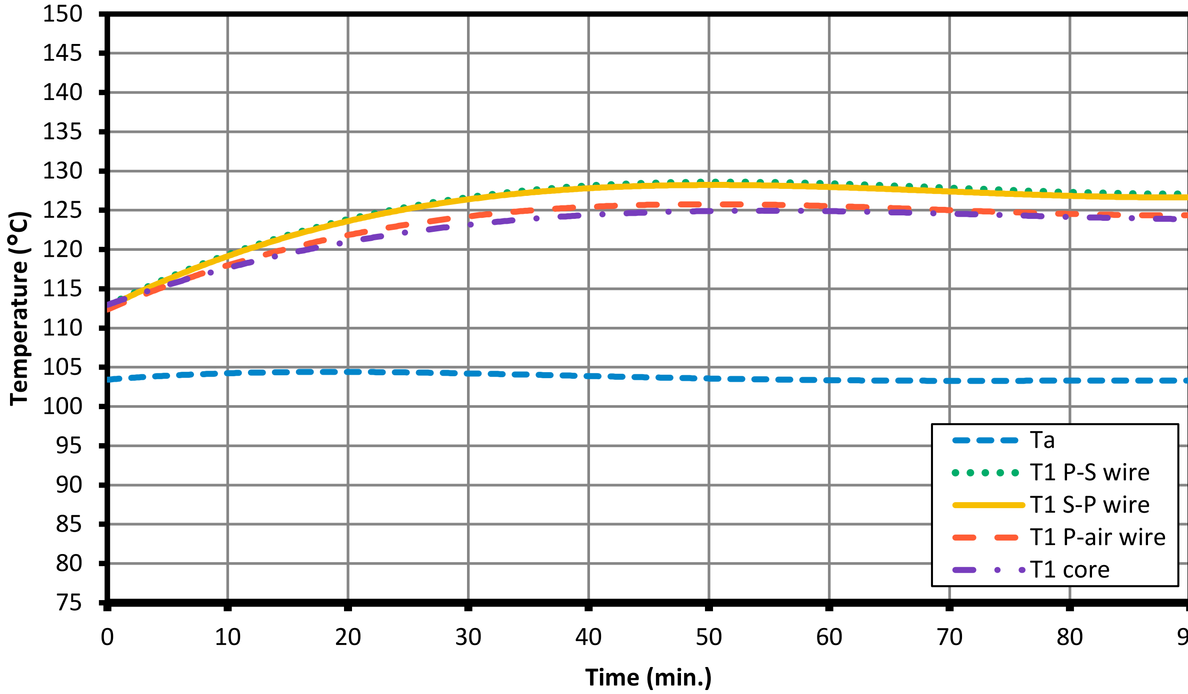


Figure 53 – 1000 V_{DC} Input, 13 W Output Operating Temperature of DER-956Q T1 Flyback Transformer.

10.2 *Thermal Data at 25 °C Ambient Temperature*

The following thermal scans were captured using Fluke thermal imager after soaking the unit under test for at least one (1) hour in an acrylic enclosure to minimize the effect on any external/forced air flow.

Critical Components	Input Voltage			
	30 V	60 V	800 V	1000 V
Input CMC	43.6 °C	47.2 °C	68.9 °C	77.3 °C
Transformer Core	40.6 °C	44.3 °C	49.6 °C	52.5 °C
Transformer Wire	42.0 °C	46.5 °C	51.6 °C	54.4 °C
18 V SR FET	37.6 °C	40.5 °C	47.0 °C	50.0 °C
Secondary Snubber Resistor	37.3 °C	39.9 °C	48.2 °C	51.9 °C
18 V Cout	36.0 °C	40.6 °C	44.7 °C	44.4 °C
18 V Cfilter	35.6 °C	38.0 °C	41.7 °C	42.7 °C
9 V Freewheeling Diode	50.7 °C	51.0 °C	53.5 °C	55.3 °C
Primary Snubber Resistor	50.8 °C	57.0 °C	59.7 °C	62.3 °C
INN3949CQ	42.6 °C	46.1 °C	58.7 °C	66.5 °C
Ambient Temperature	31.0 °C	30.0 °C	30.8 °C	31.2 °C

Table 9 – Summary of DER-956Q Critical Components 25 °C Operating Temperature.

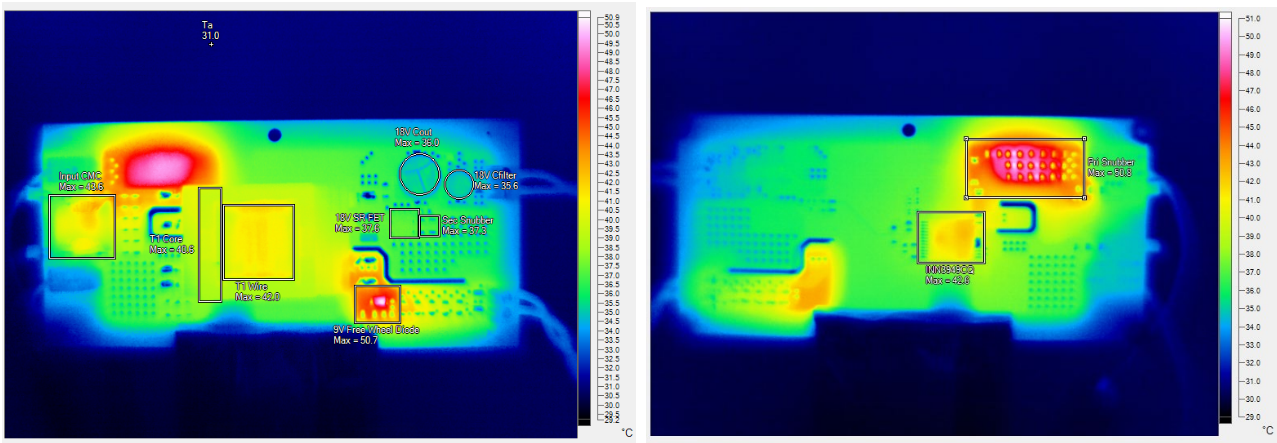


Figure 54 – 30 V_{DC} Input, 13 W Output Thermal Scans, Top PCB (Left) and Bottom PCB (Right).

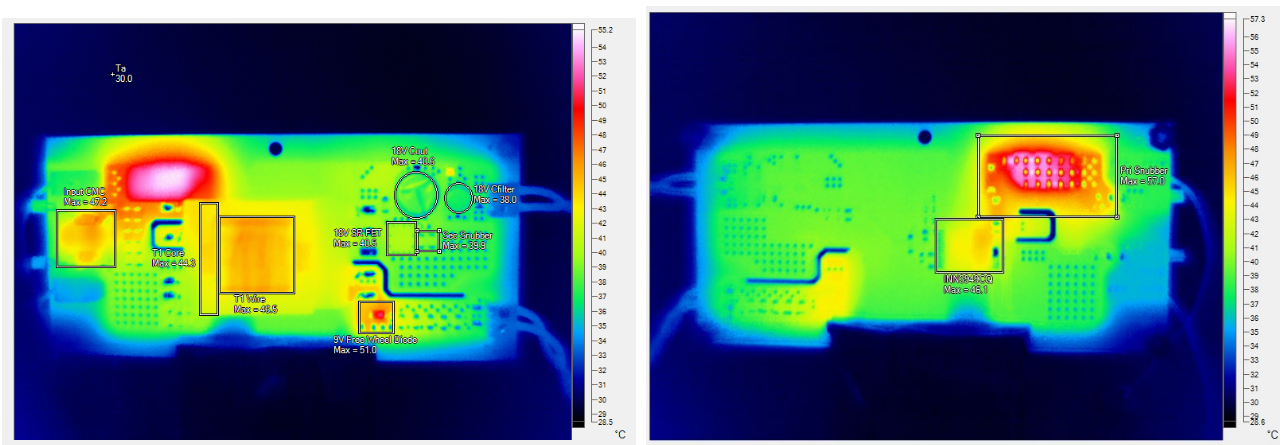


Figure 55 – 60 V_{DC} Input, 13 W Output Thermal Scans, Top PCB (Left) and Bottom PCB (Right)

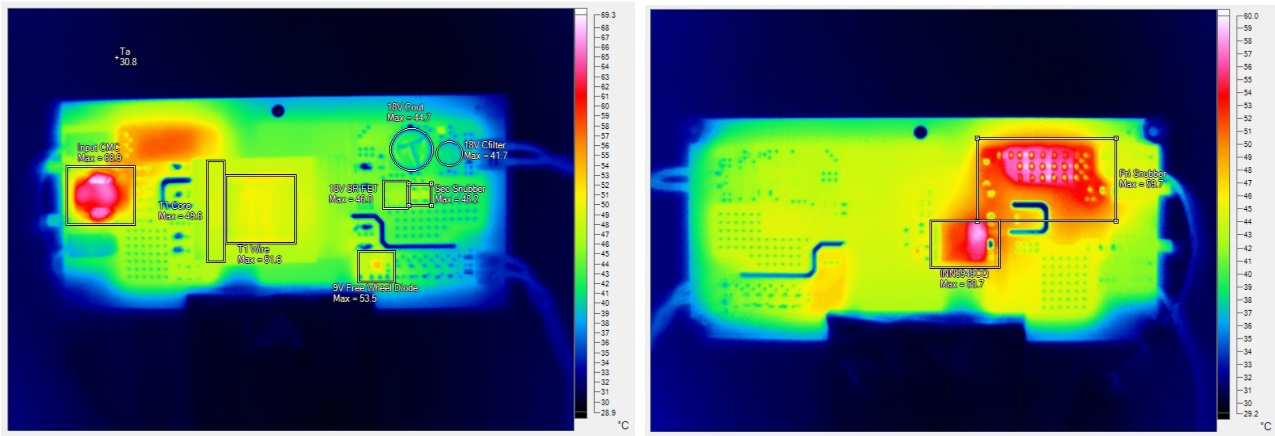


Figure 56 – 800 V_{DC} Input, 13 W Output Thermal Scans, Top PCB (Left) and Bottom PCB (Right).

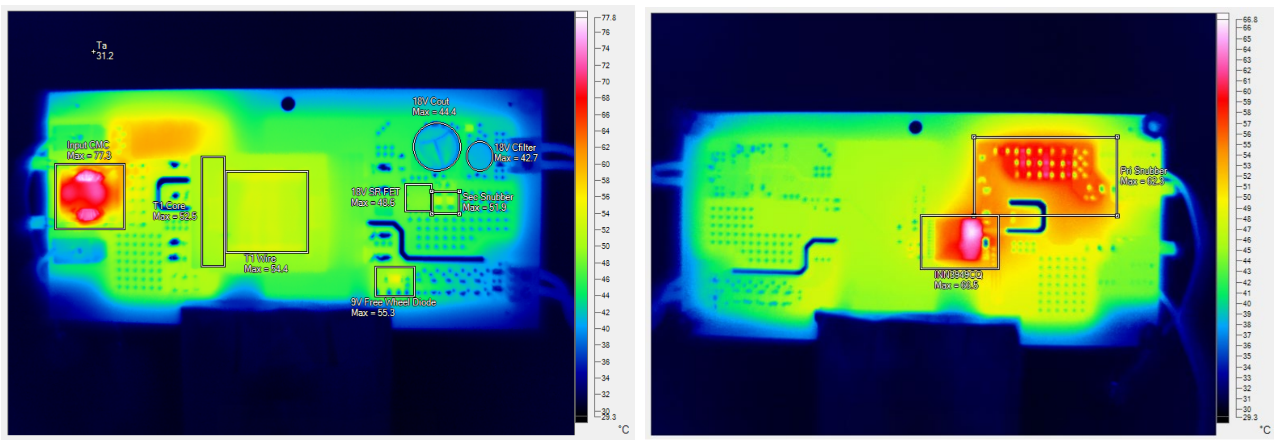


Figure 57 – 1000 V_{DC} Input, 13 W Output Thermal Scans, Top PCB (Left) and Bottom PCB (Right).

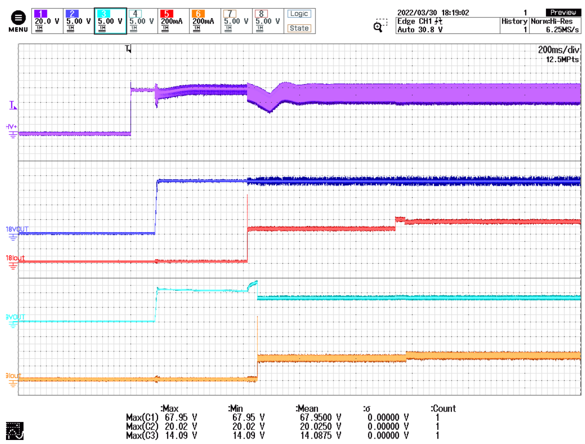
11 Waveforms

11.1 *Start-up Waveforms*

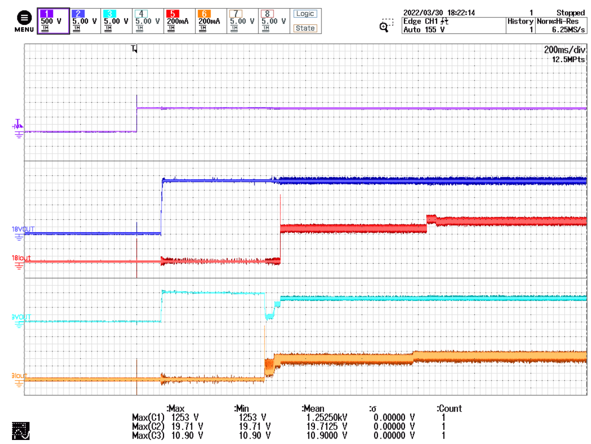
11.1.1 25 °C Ambient Temperature

The following measurements were taken by hot plugging-in the unit under test to a DC link capacitor fully charged[23] to a test input voltage of HV+.

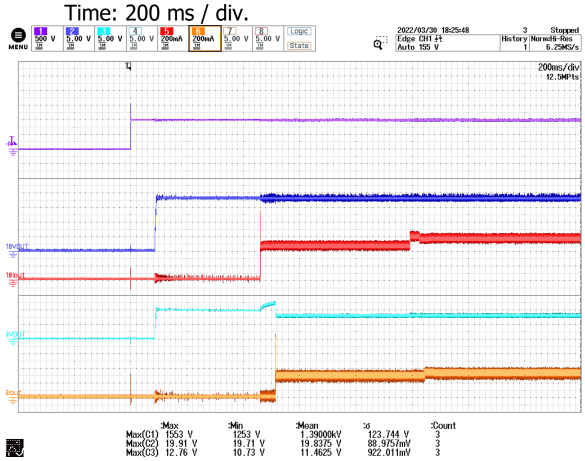
11.1.1.1 Output Voltage and Current[24,25]



a. CH1: HV+, 20 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.



b. CH1: HV+, 500 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.



c. CH1: HV+, 500 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.

Figure 58 – Output Voltage and Current.

a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

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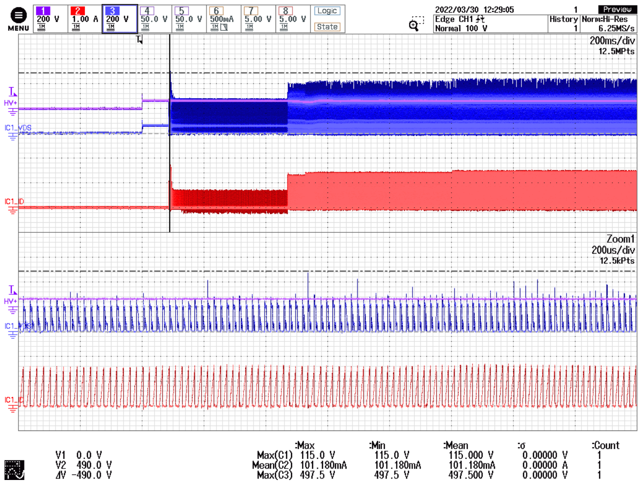
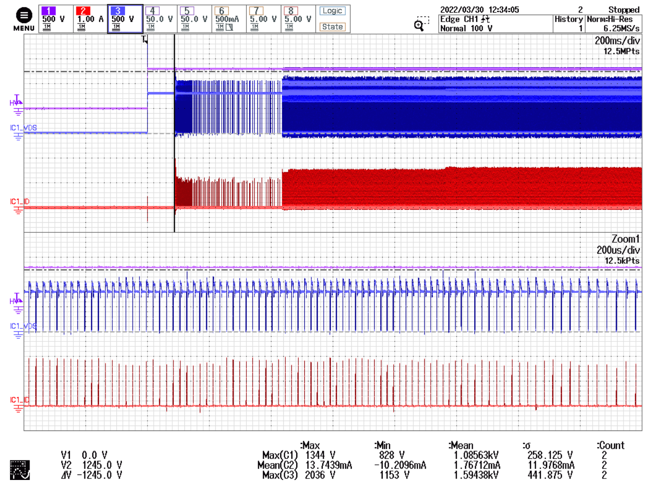
[23] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[24] Voltage dip on the HV+ waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[25] The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between the output voltages and output current rising edge is also due to the electronic load response.

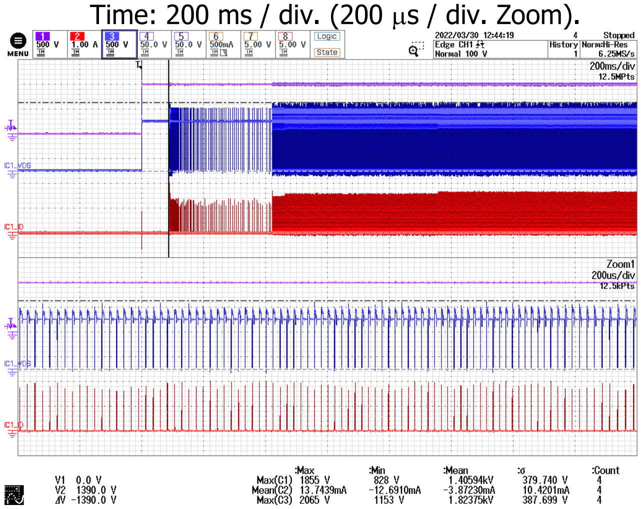
11.1.1.2 Primary Drain Voltage and Current[26,27]



a. CH1: HV+, 200 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 200 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).

Figure 59 – Primary Drain Voltage and Current.

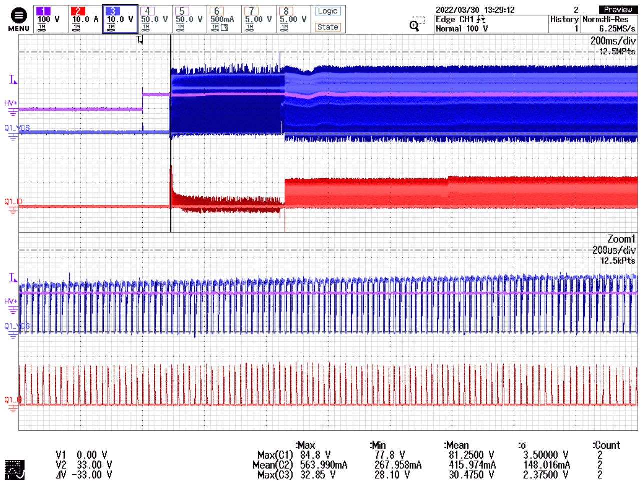
a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

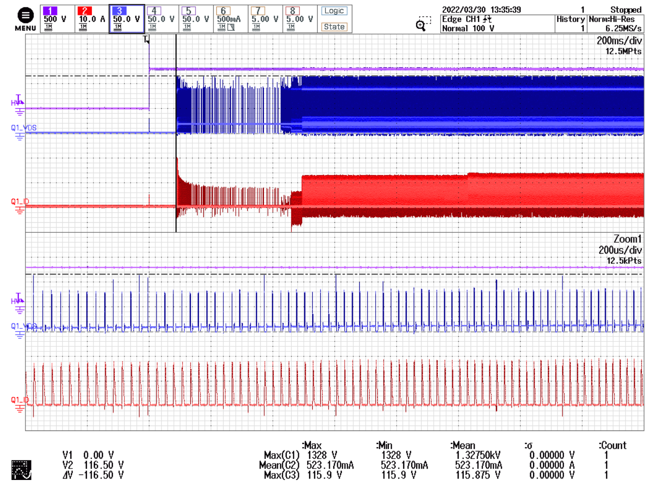
c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

[26] The time between when HV+ is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[27] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

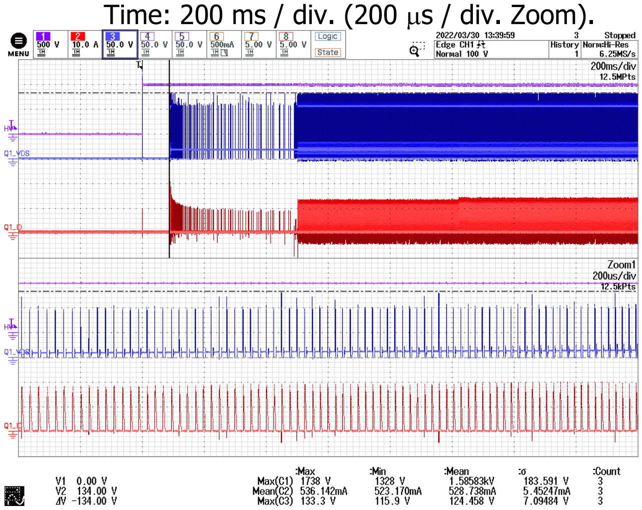
11.1.1.3 SR FET Drain Voltage and Current[28,29]



a. CH1: HV+, 100 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 10 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 50 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 50 V / div.
Time: 200 ms / div. (200 μs / div. Zoom).

Figure 60 – SR FET Drain Voltage and Current.

a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

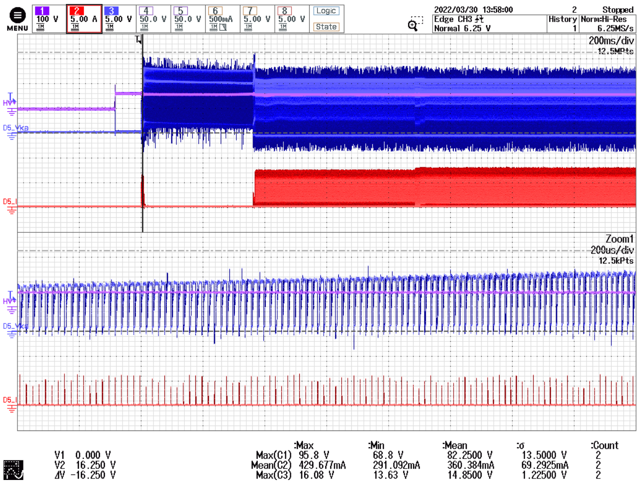
b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

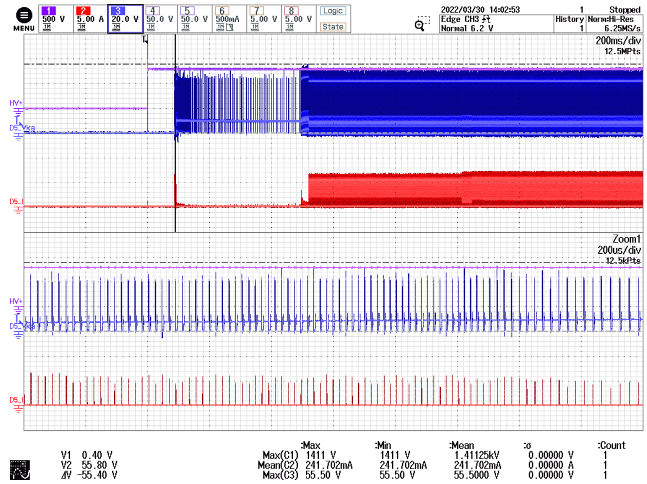
[28] The time between when HV+ is turned on and the SR FET starts switching is due to the "Wait and Listen" period of the InnoSwitch.

[29] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

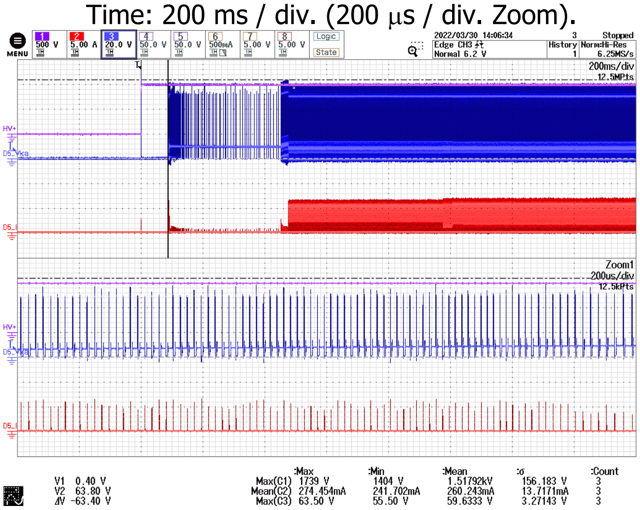
11.1.1.4 9 V Output Diode Voltage and Current[30,31]



a. CH1: HV+, 100 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 5 V / div.
Time: 200 ms / div. (200 µs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 20 V / div.
Time: 200 ms / div. (200 µs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 20 V / div.
Time: 200 ms / div. (200 µs / div. Zoom).

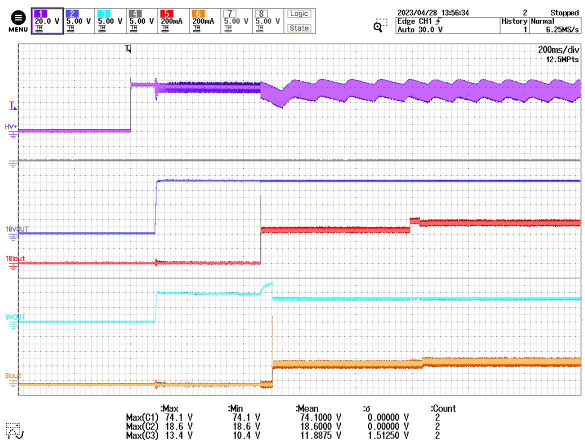
Figure 61 – 9 V Freewheeling Diode Voltage and Current.

a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

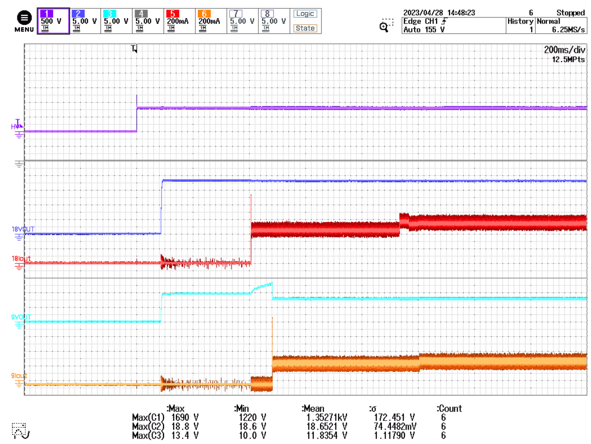
[30] The time between when HV+ is turned on and the 9 V output diode starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[31] The change in the switching frequency of the 9 V output diode is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.2 - 40 °C Ambient Temperature

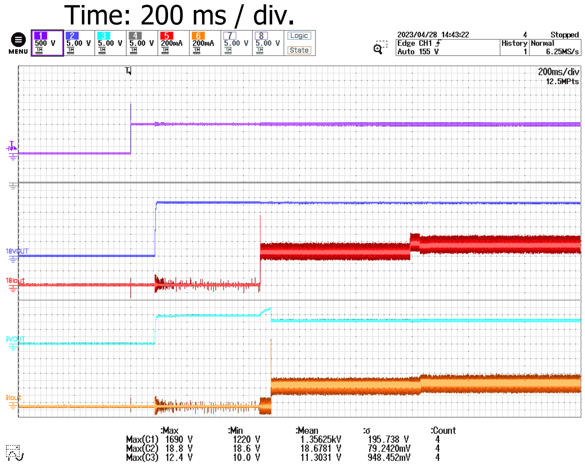
11.1.2.1 Output Voltage and Current[32,33]



d. CH1: HV+, 20 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.



e. CH1: HV+, 500 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.



f. CH1: HV+, 500 V / div.
CH2: 18 V, 5 V / div.
CH3: 9 V, 5 V / div.
CH5: 18 V I_{OUT}, 200 mA / div.
CH6: 9 V I_{OUT}, 200 mA / div.
Time: 200 ms / div.

Figure 62 – Output Voltage and Current.

d. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

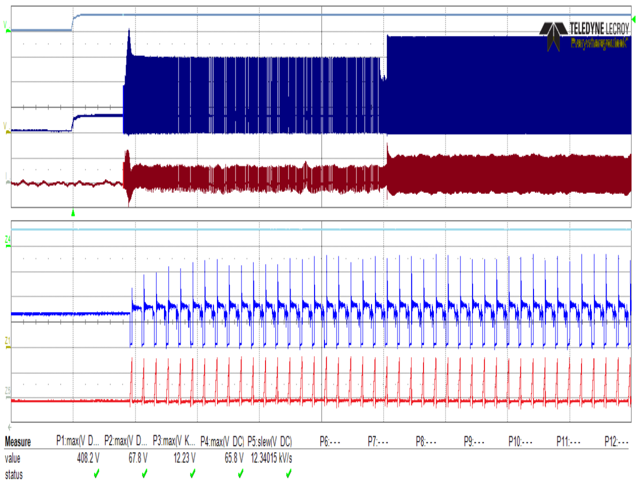
e. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

f. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

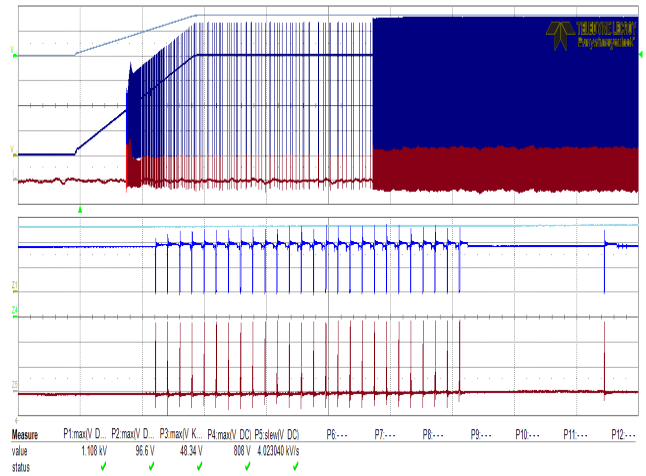
32 Voltage dip on the HV+ waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
33 The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between the output voltages and output current rising edge is also due to the electronic load response.

The following measurements were taken using a DC link voltage rise time of 500 ns (10% to 90% of HV+ within 500 ns).

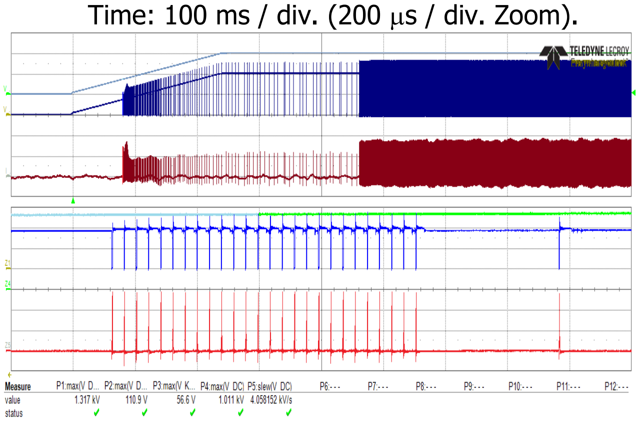
11.1.2.2 Primary Drain Voltage and Current[34,35]



a. CH1: HV+, 100 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 100 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 200 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).

Figure 63 – Primary Drain Voltage and Current.

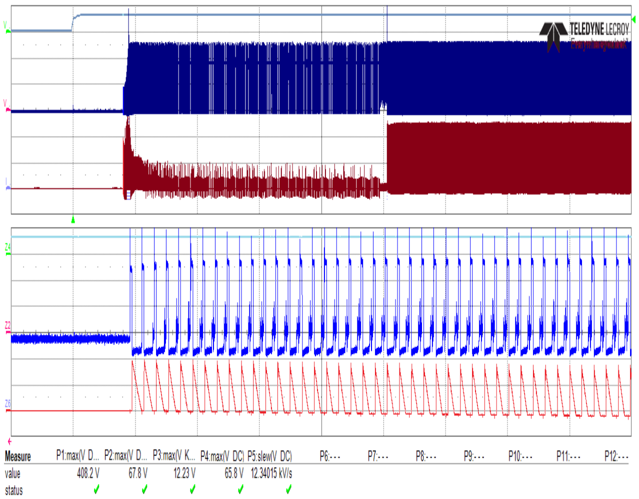
a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

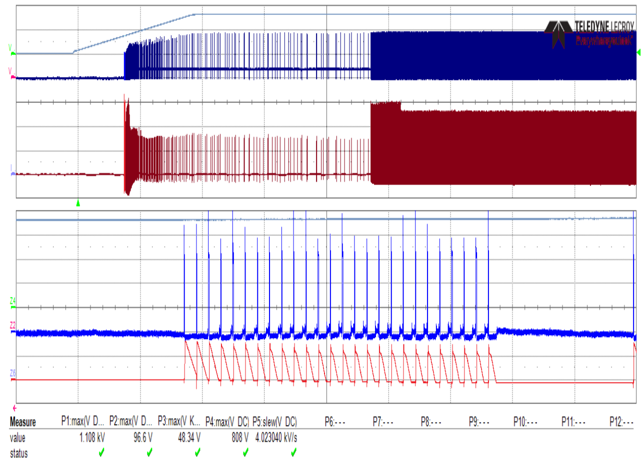
c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

[34] The time between when HV+ is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[35] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

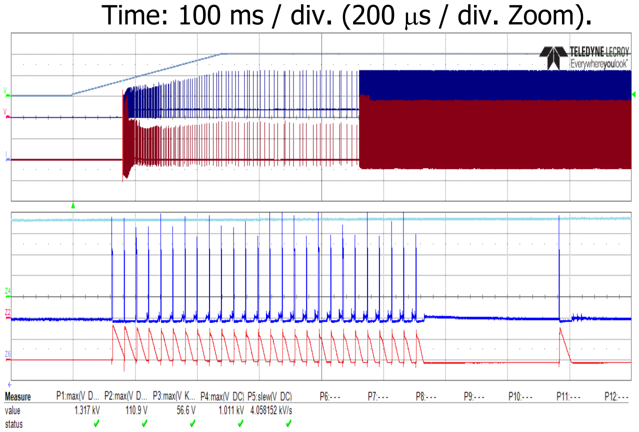
11.1.2.3 SR FET Drain Voltage and Current[36,37]



a. CH1: HV+, 100 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 10 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{DS}, 50 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{DS}, 50 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).

Figure 64 – SR FET Drain Voltage and Current.

a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

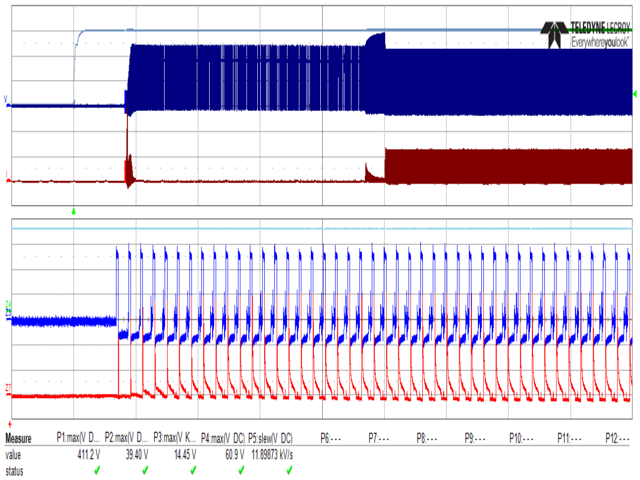
b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

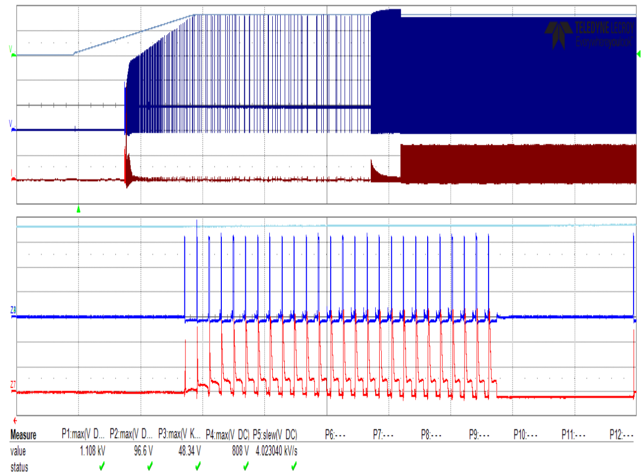
[36] The time between when HV+ is turned on and the SR FET starts switching is due to the "Wait and Listen" period of the InnoSwitch.

[37] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

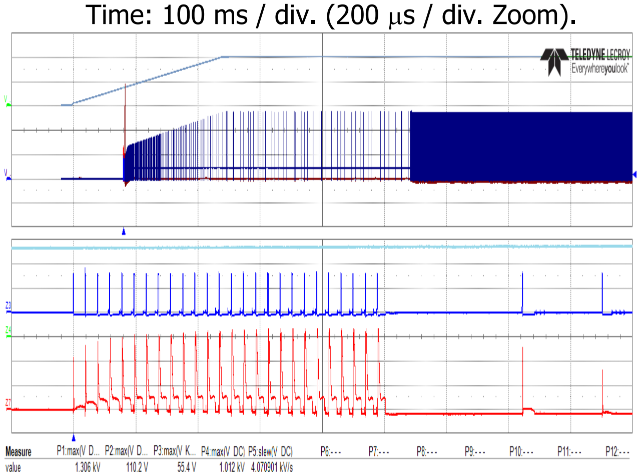
11.1.2.4 9 V Output Diode Voltage and Current[38,39]



a. CH1: HV+, 20 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 5 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



b. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 10 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).



c. CH1: HV+, 500 V / div.
CH2: I_D, 5 A / div.
CH3: V_{KA}, 20 V / div.
Time: 100 ms / div. (200 µs / div. Zoom).

Figure 65 – 9 V Freewheeling Diode Voltage and Current.

a. 60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
b. 800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
c. 1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.

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38 The time between when HV+ is turned on and the 9 V output diode starts switching is due to the "Wait and Listen" period of the InnoSwitch.
39 The change in the switching frequency of the 9 V output diode is due to the CR (Constant Resistance) mode response of the electronic load.

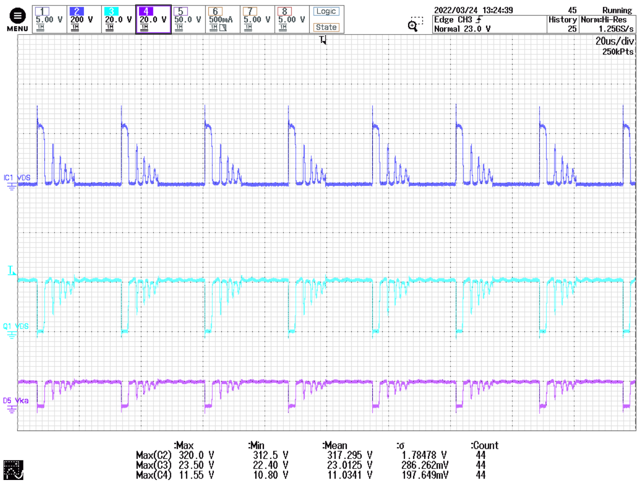
11.2 *Steady-State Stress Waveforms*

11.2.1 Switching Waveforms at 105 °C Ambient Temperature

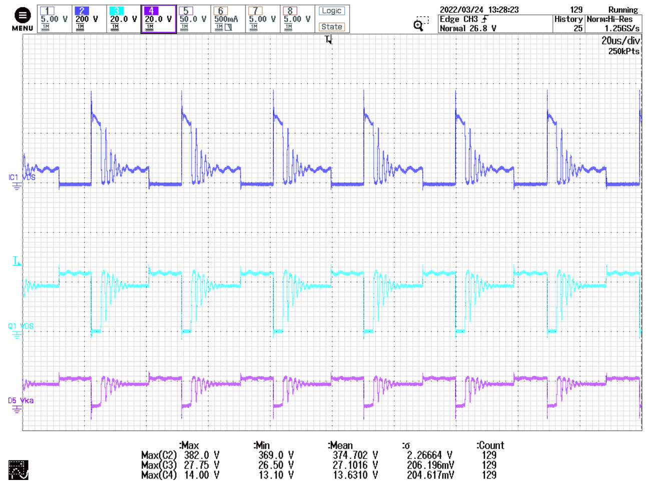
11.2.1.1 Normal Condition

Steady-State Switching Waveforms 105 °C Ambient Temperature								
Input	**18 V Output**	**9 V Output**	**INN3949CQ**		**18 V SR FET**		**9 V Freewheeling Diode**	
V_{IN} (V)	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**IC1 V_{DS} (V)**	**V_{STRESS} (%)**	**Q1 V_{DS} (V)**	**V_{STRESS} (%)**	**D5 (V_{KA})**	**V_{STRESS} (%)**
30	222	22	323	19.00	23.15	15.00	12.4	12.00
	166	333	318	19.00	23.2	15.00	11.1	11.00
	222	333	320	19.00	23.5	16.00	11.55	12.00
60	555	22	391	23.00	27.3	18.00	16.05	16.00
	166	333	350.5	21.00	27.2	18.00	13.25	13.00
	555	333	382	22.00	27.75	19.00	14	14.00
800	555	22	1090	64.00	111.5	74.00	59.5	60.00
	166	333	1080	64.00	111.8	75.00	57	57.00
	555	333	1140	67.00	112.1	75.00	57.5	58.00
1000	555	22	1301	77.00	120.5	80.00	69.5	70.00
	166	333	1270	75.00	122.6	82.00	66.4	66.00
	555	333	1299	76.00	120	80.00	68.5	69.00

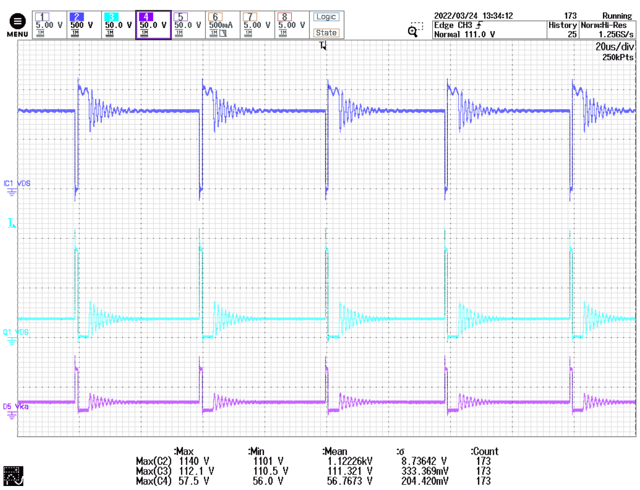
Table 10 – Summary of Voltage Stress Analysis at 105 °C Ambient Temperature.



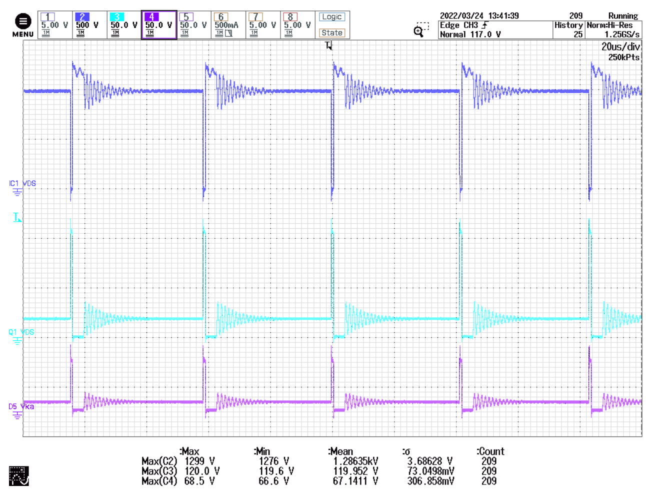
30 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 200 V / div.
CH3: SR FET V_{DS}, 20 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 20 V / div.
Time: 20 µs / div.



60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 200 V / div.
CH3: SR FET V_{DS}, 20 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 20 V / div.
Time: 20 µs / div.



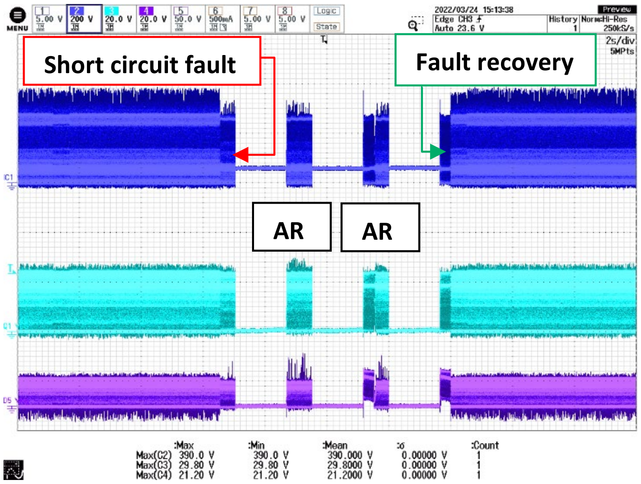
800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 500 V / div.
CH3: SR FET V_{DS}, 50 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 50 V / div.
Time: 20 µs / div.



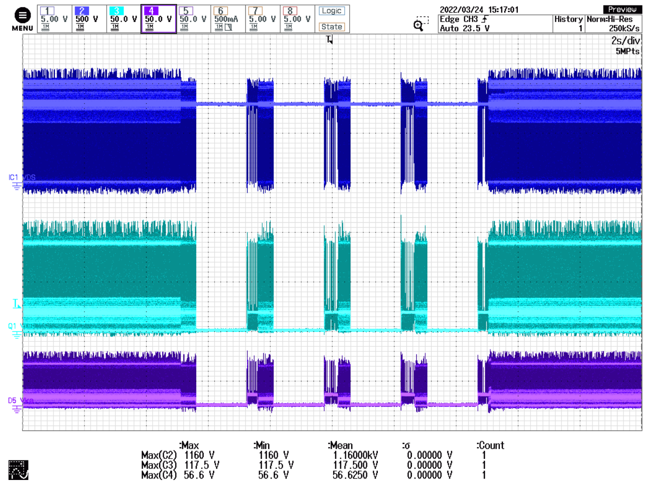
1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 500 V / div.
CH3: SR FET V_{DS}, 50 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 50 V / div.
Time: 20 µs / div.

Figure 66 – Switching Waveforms During Normal Condition at 105 °C Ambient Temperature.

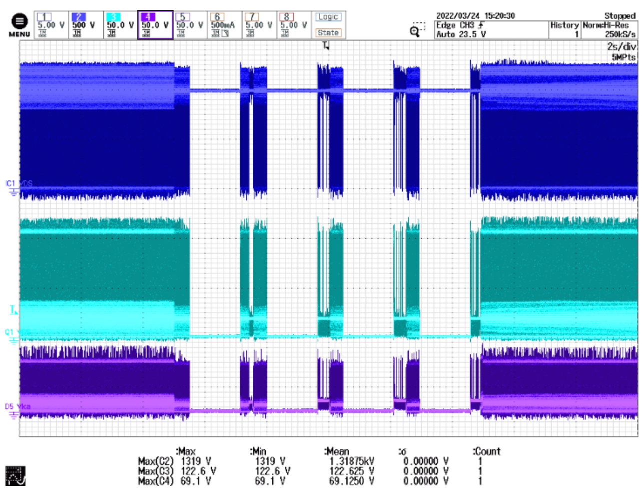
11.2.1.2 Short-Circuit Response



60 V_{DC} Input,
18 V = Max.-Short-Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 200 V / div.
CH3: SR FET V_{DS}, 20 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 20 V / div.
Time: 2 s / div.



800 V_{DC} Input,
18 V = Max.-Short-Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 500 V / div.
CH3: SR FET V_{DS}, 50 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 50 V / div.
Time: 2 s / div.



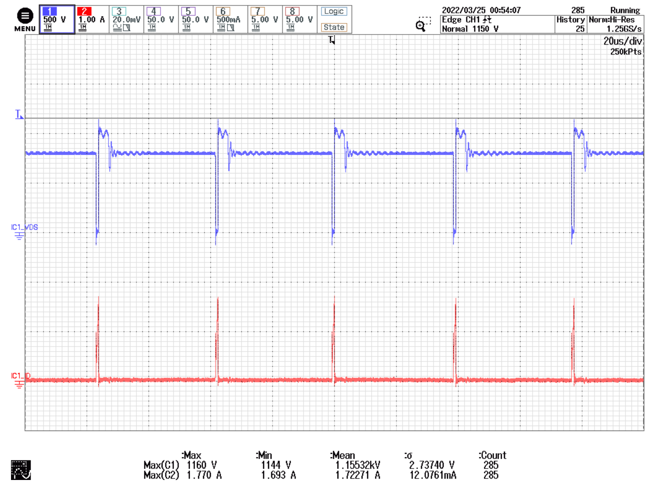
1000 V_{DC} Input,
18 V = Max.-Short-Max. 9 V = Max. Output.
CH2: INN3949CQ V_{DS}, 500 V / div.
CH3: SR FET V_{DS}, 50 V / div.
CH4: 9 V Freewheeling Diode V_{KA}, 50 V / div.
Time: 2 s / div.

Figure 67 – Switching Waveforms During Short-Circuit Condition at 105 °C Ambient Temperature.

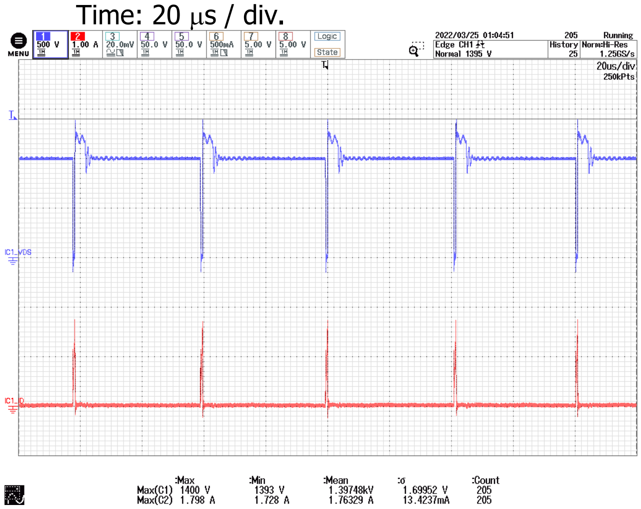
11.2.2 Switching Waveforms at 25 °C Ambient Temperature

11.2.2.1 Primary Drain Voltage and Current

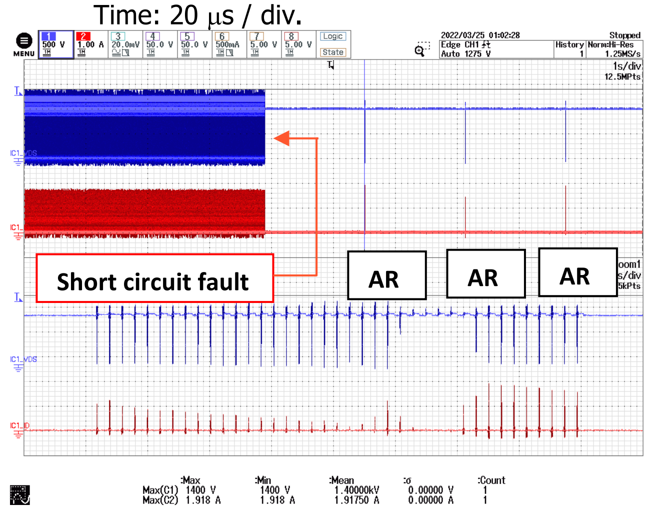
60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 200 V / div.
CH2: I_D, 1 A / div.
Time: 20 μs / div.



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 500 V / div.
CH2: I_D, 1 A / div.
Time: 20 μs / div.



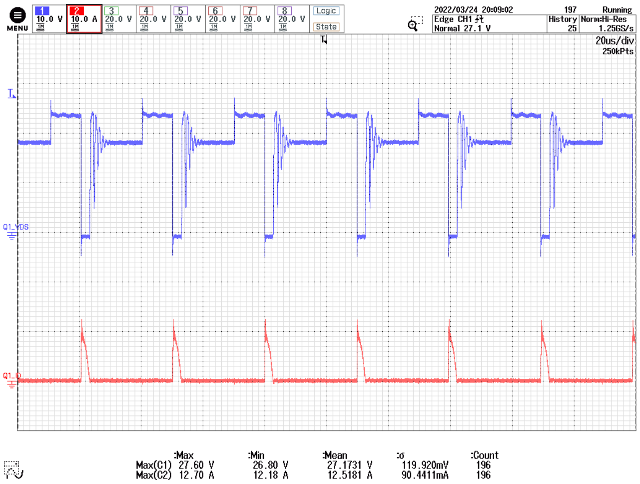
1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 500 V / div.
CH2: I_D, 1 A / div.
Time: 20 μs / div.



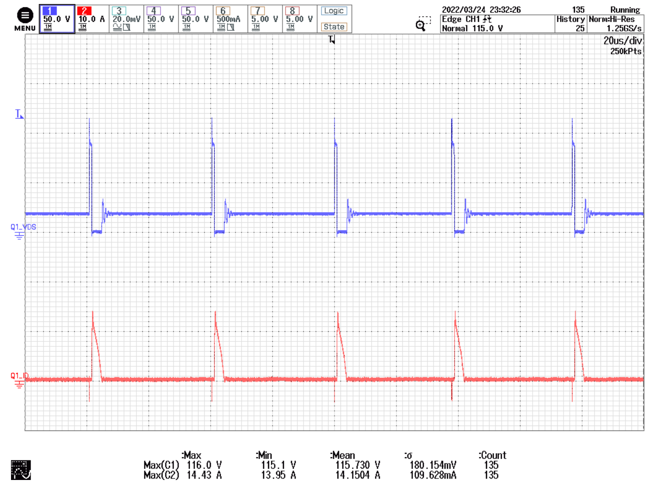
1000 V_{DC} input, 18 V = Max.-Short 9 V = Max. Output.
CH1: V_{DS}, 500 V / div.
CH2: I_D, 1 A / div.
Time: 1 s / div. (200 μs / div. Zoom).

Figure 68 – Primary Drain Voltage and Current at 25 °C Ambient Temperature.

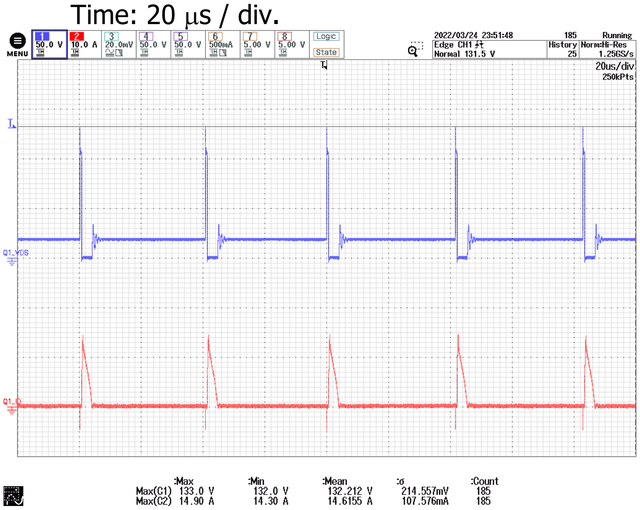
11.2.2.2 SR FET Drain Voltage and Current



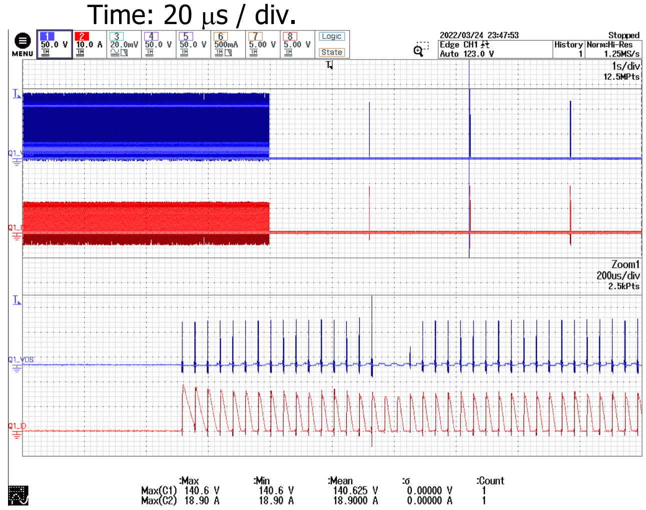
60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 10 V / div.
CH2: I_D, 10 A / div.
Time: 20 µs / div.



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 50 V / div.
CH2: I_D, 10 A / div.
Time: 20 µs / div.



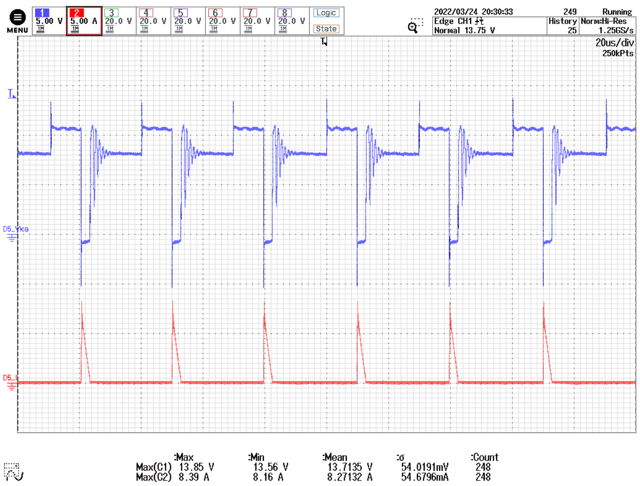
1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{DS}, 50 V / div.
CH2: I_D, 10 A / div.
Time: 20 µs / div.



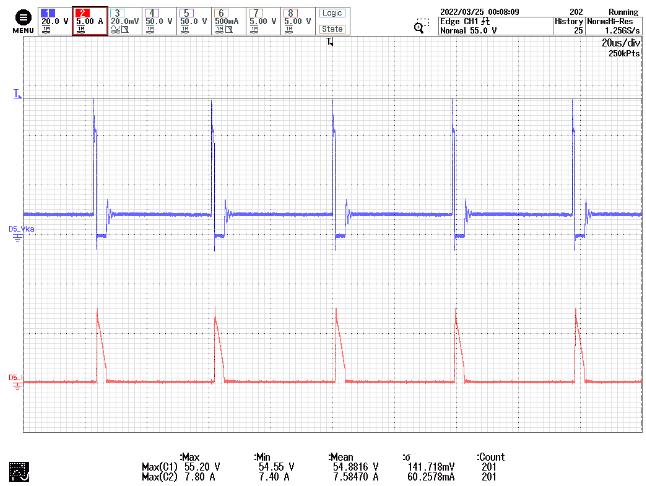
1000 V_{DC} Input, 18 V = Max.-Short 9 V = Max. Output.
CH1: V_{DS}, 50 V / div.
CH2: I_D, 10 A / div.
Time: 1 s / div. (200 µs / div. Zoom).

Figure 69 – SR FET Drain Voltage and Current at 25 °C Ambient Temperature.

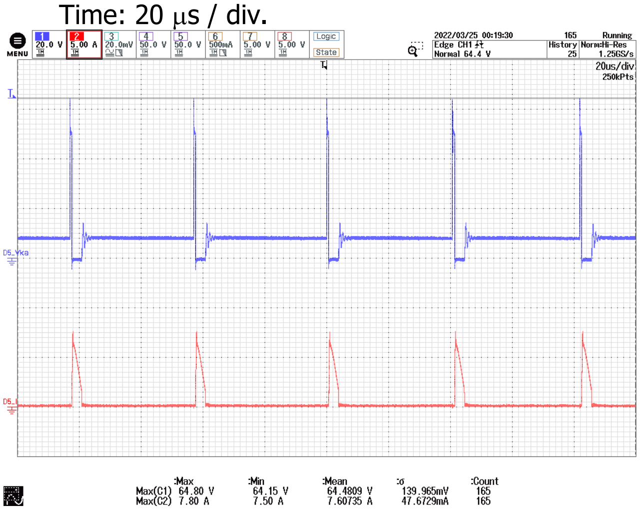
11.2.2.3 9 V Freewheeling Diode Voltage and Current



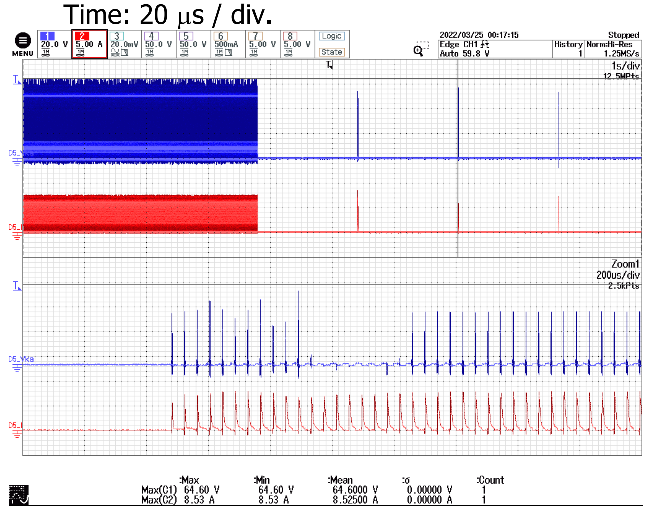
60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{KA}, 5 V / div.
CH2: I_D, 5 A / div.
Time: 20 µs / div.



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{KA}, 20 V / div.
CH2: I_D, 5 A / div.
Time: 20 µs / div.



1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: V_{KA}, 20 V / div.
CH2: I_D, 5 A / div.
Time: 20 µs / div.



1000 V_{DC} Input, 18 V = Max.-Short 9 V = Max. Output.
CH1: V_{KA}, 20 V / div.
CH2: I_D, 5 A / div.
Time: 1 s / div. (200 µs / div. Zoom).

Figure 70 – 9 V Freewheeling Diode Voltage and Current at 25 °C Ambient Temperature.

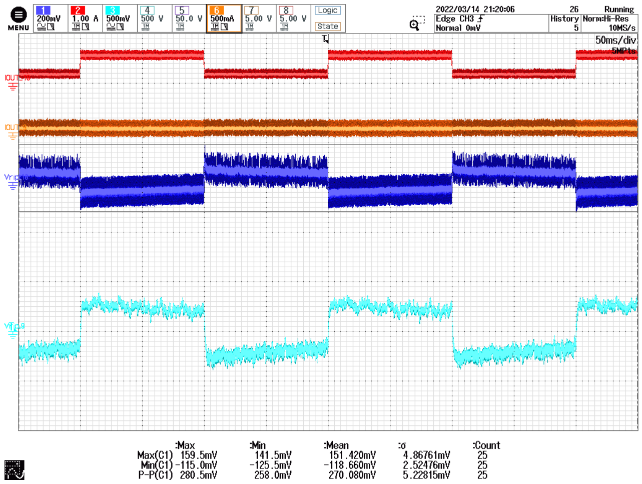
11.3 *Load Transient Response*

Load transient response describes the response characteristic of the unit under test to sudden load changes. Output voltage waveforms on the unit were captured with switching load transient from minimum to maximum and back to minimum. Duration for load state high is 100 ms and for low is 100 ms with a slew rate of 100 mA / µs.

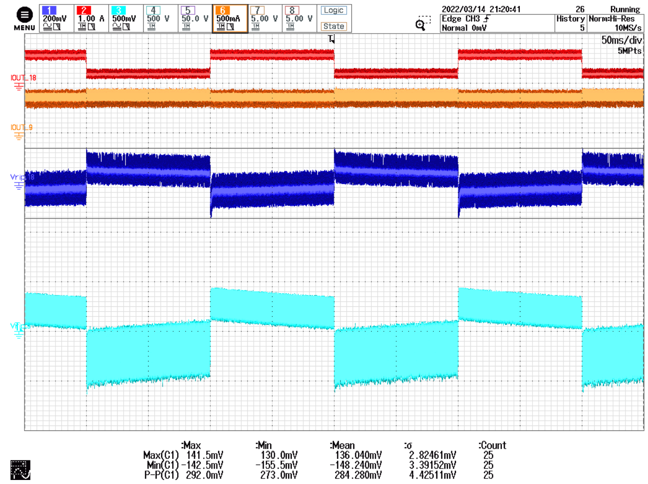
11.3.1 Load Transient Response at 105 °C Ambient Temperature

Test Conditions (0.1 A / µs Slew Rate, 200 ms Period, Min.-Typ.-Min.)			**Output Overshoot and Undershoot Results**			
Input	**18 V Output**	**9 V Output**	**18 V output**		**9 V Output**	
V_{IN} (V)	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**18 V_{MAX}**	**18 V_{MIN}**	**9 V_{MAX}**	**9 V_{MIN}**
30	switching	22.00	18.02	17.96	8.62	8.24
	switching	333.00	18.07	17.91	8.64	8.15
	166.00	switching	18.04	17.94	9.00	7.52
	222.00	switching	18.06	17.92	9.09	7.56
60	switching	22.00	18.07	17.82	9.33	8.11
	switching	333.00	18.06	17.85	9.11	8.11
	166.00	switching	18.00	17.93	9.32	7.79
	555.00	switching	18.00	17.94	9.56	7.80
800	switching	22.00	18.14	17.91	9.01	8.01
	switching	333.00	18.14	17.88	8.94	7.84
	166.00	switching	18.10	17.97	9.19	7.47
	555.00	switching	18.08	17.98	9.21	7.72
1000	switching	22.00	18.19	17.90	8.90	8.05
	switching	22.00	18.17	17.87	8.92	7.82
	166.00	switching	18.12	17.97	9.15	7.36
	555.00	switching	18.11	17.95	9.13	7.75

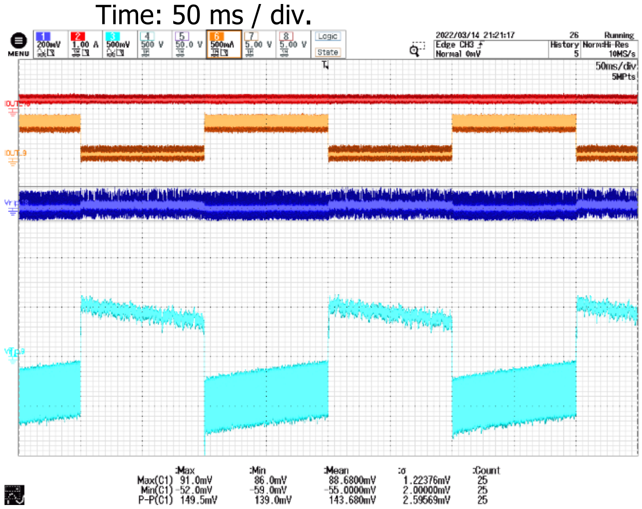
Table 11 – Summary of Load Transient Response at 105 °C Ambient.



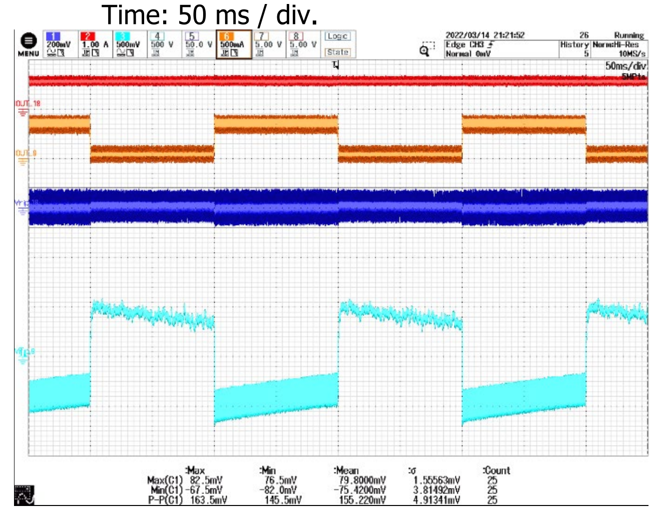
Load: 18 V = Switching 9 V = Min. Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



Load: 18 V = Switching 9 V = Max. Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



Load: 18 V = Min. 9 V = Switching Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



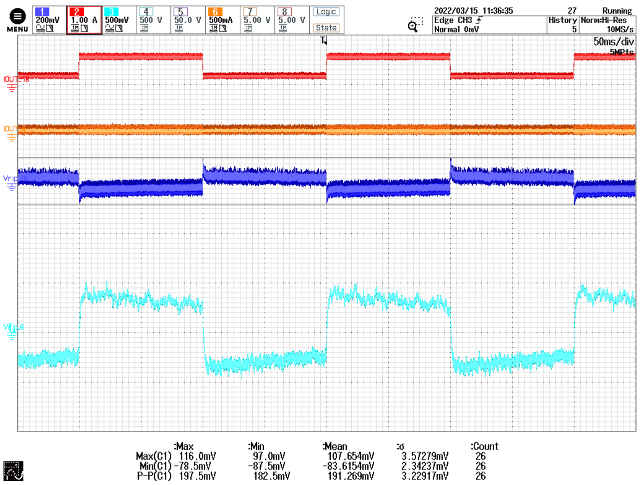
Load: 18 V = Max. 9 V = Switching Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.

Figure 71 – 1000 V_{DC} Input Load Transient Response at 105 °C Ambient Temperature.

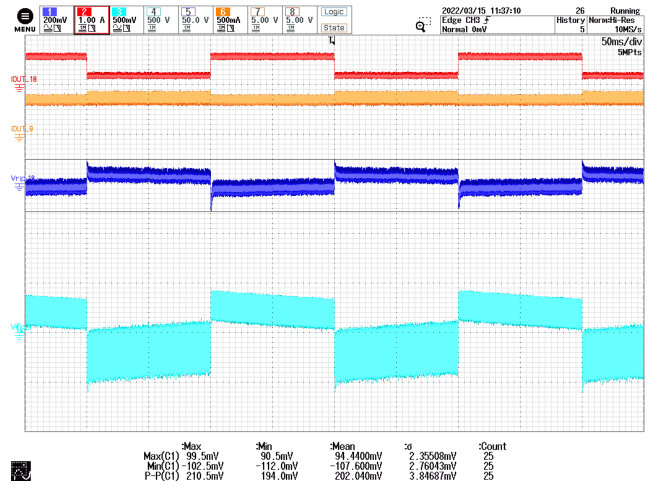
11.3.2 Load Transient Response 25 °C Ambient Temperature

Test Conditions (0.1 A / µs Slew Rate, 200 ms Period, Min.-Typ.-Min.)			**Output Overshoot and Undershoot Results**			
Input	**18 V Output**	**Input**	**18 V Output**		**Input**	
V_{IN} (V)	**I_{OUT} (mA)**	**V_{IN} (V)**	**I_{OUT} (mA)**	**V_{IN} (V)**	**I_{OUT} (mA)**	**V_{IN} (V)**
30	switching	22.00	18.06	18.00	8.39	8.04
	switching	333.00	18.10	17.96	8.42	7.96
	166.00	switching	18.07	17.97	8.78	7.34
	222.00	switching	18.10	17.93	8.82	7.41
60	switching	22.00	18.11	17.89	9.23	7.99
	switching	333.00	18.10	17.92	8.99	8.03
	166.00	switching	18.04	17.98	9.20	7.71
	555.00	switching	18.05	17.99	9.47	7.71
800	switching	22.00	18.18	18.00	8.93	7.85
	switching	333.00	18.17	17.97	8.81	7.74
	166.00	switching	18.14	18.06	9.05	7.52
	555.00	switching	18.12	18.06	9.16	7.56
1000	switching	22.00	18.19	17.98	8.89	7.86
	switching	22.00	18.17	17.96	8.80	7.75
	166.00	switching	18.13	18.04	9.03	7.31
	555.00	switching	18.12	18.03	9.13	7.56

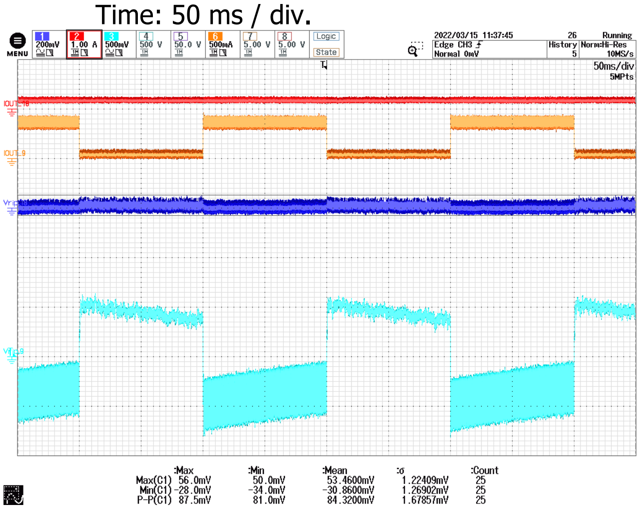
Table 12 – Summary of Load Transient Response at 25 °C Ambient.



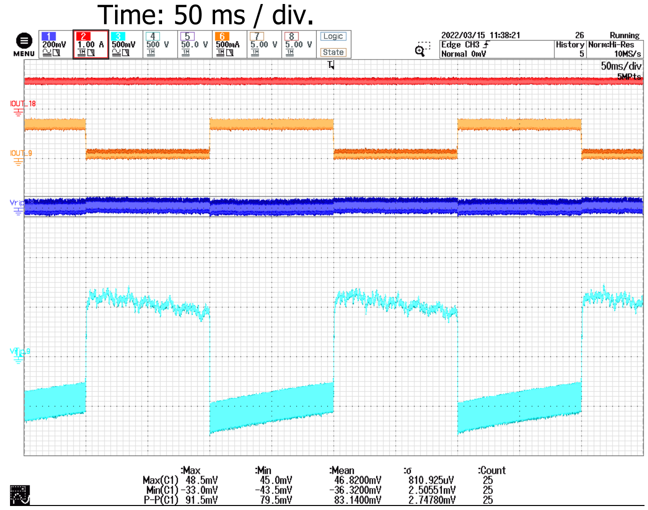
Load: 18 V = Switching 9 V = Min. Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



Load: 18 V = Switching 9 V = Max. Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



Load: 18 V = Min. 9 V = Switching Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.



Load: 18 V = Max. 9 V = Switching Output.
CH1: 18 V, 200 mV / div.
CH2: 18 V I_{OUT}, 1 A / div.
CH3: 9 V, 500 mV / div.
CH6: 9 V I_{OUT}, 500 mA / div.
Time: 50 ms / div.

Figure 72 – 1000 V_{DC} Input Load Transient Response at 25 °C Ambient Temperature.

11.4 *Output Voltage Ripple Measurements*

11.4.1 Output Voltage Ripple Measurement Technique

For output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 57 and Figure 58 below.

A CT2708 probe adapter is affixed with a 1 μF, 50 V ceramic type capacitor placed in parallel across the probe tip. A twisted pair of wires kept as short as possible is soldered directly to the probe and the output terminals.

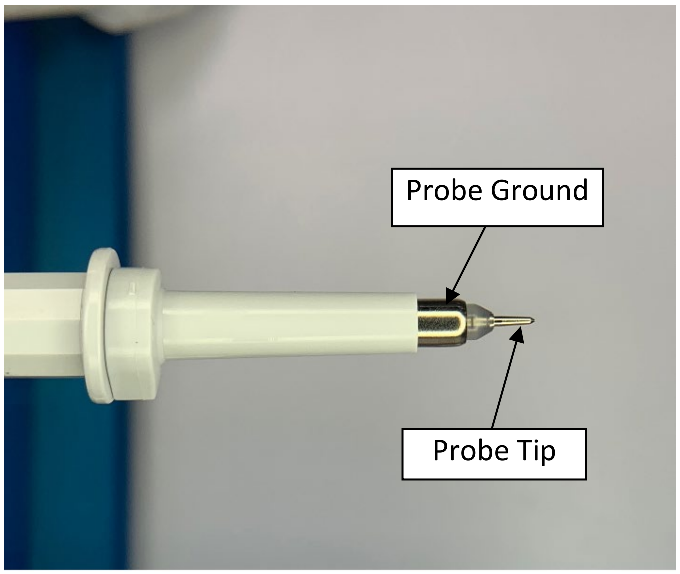


Figure 73 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

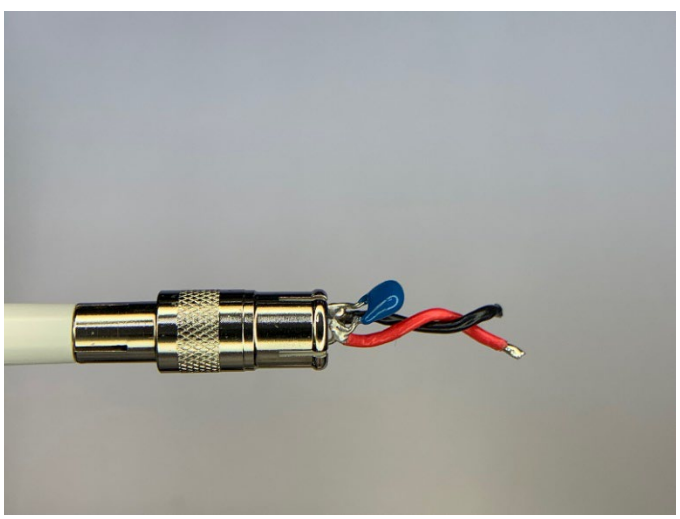
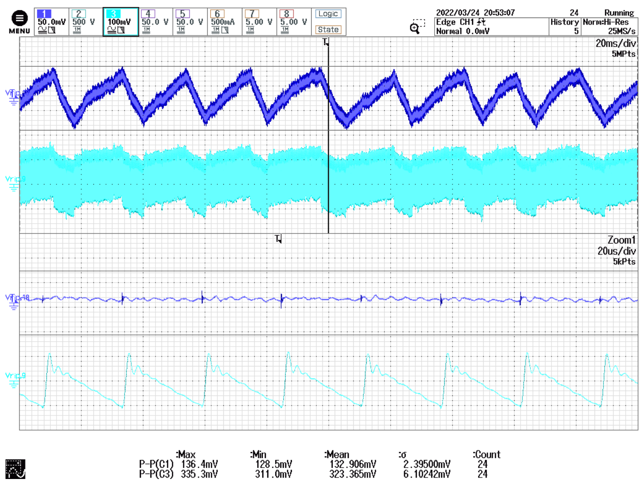


Figure 74 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with wires for ripple measurement, and a parallel decoupling capacitor added.)

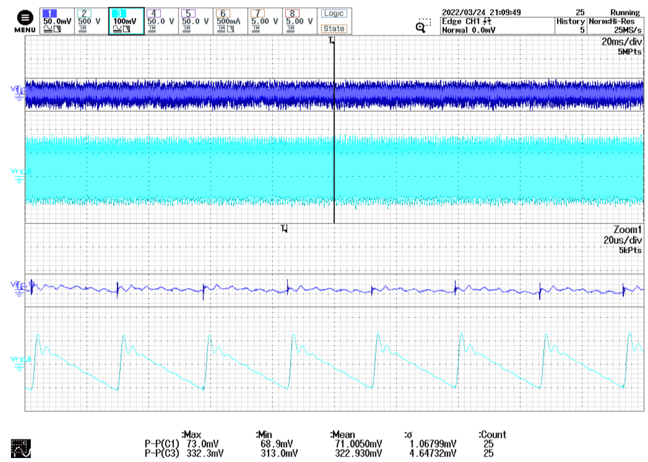
11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with decoupling capacitor. Unit under test was soaked at full load condition for at least 5 minutes for every change in the input voltage during the start of each test sequence. Also, for every loading condition, unit under test was soaked for at least 20 seconds before measurements were taken.

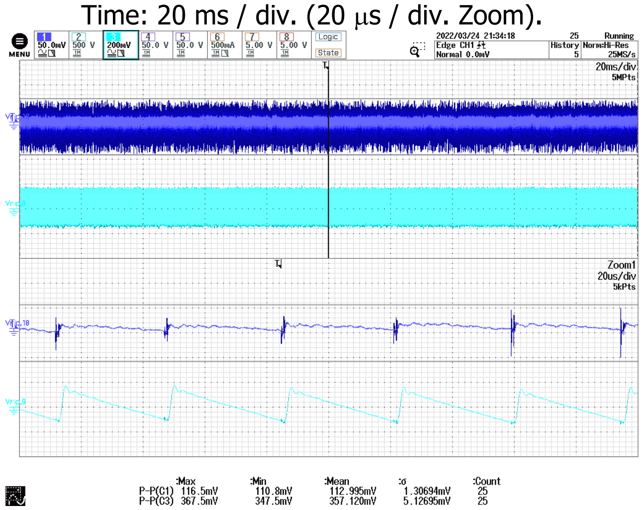
11.4.2.1 Output Voltage Ripple at 105 °C Ambient Temperature[40]



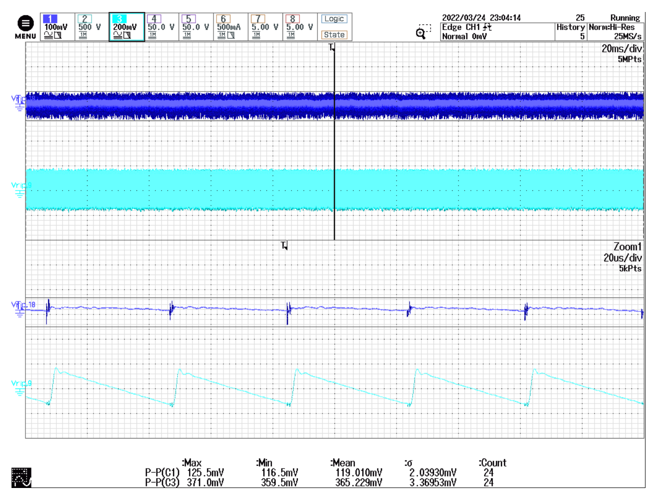
30 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (µs / div. Zoom).



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).

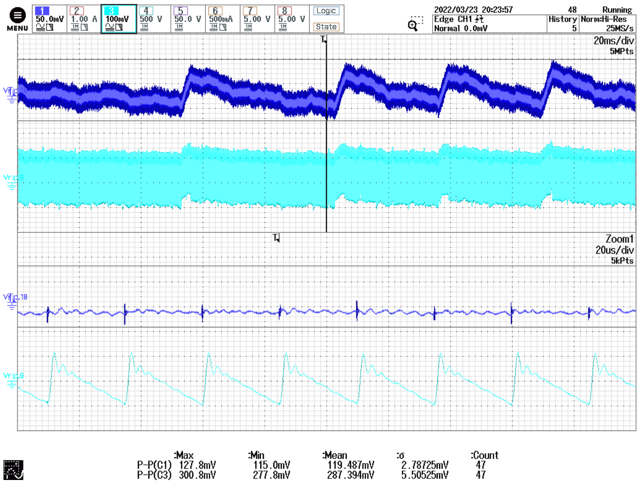


1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 100 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).

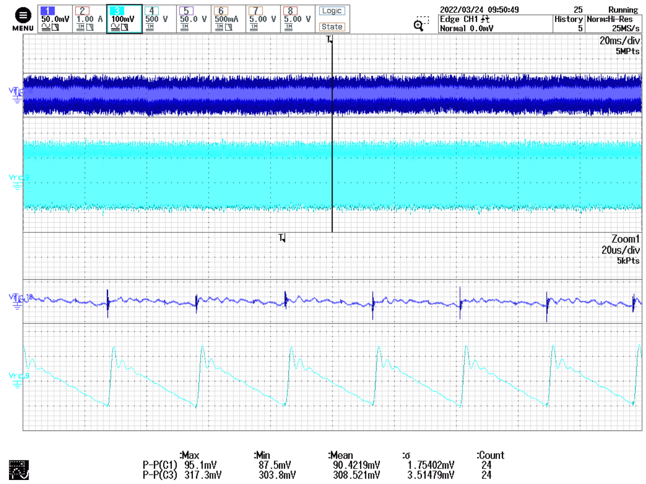
Figure 75 – Output Voltage Ripple at 105 °C Ambient Temperature.

[40] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

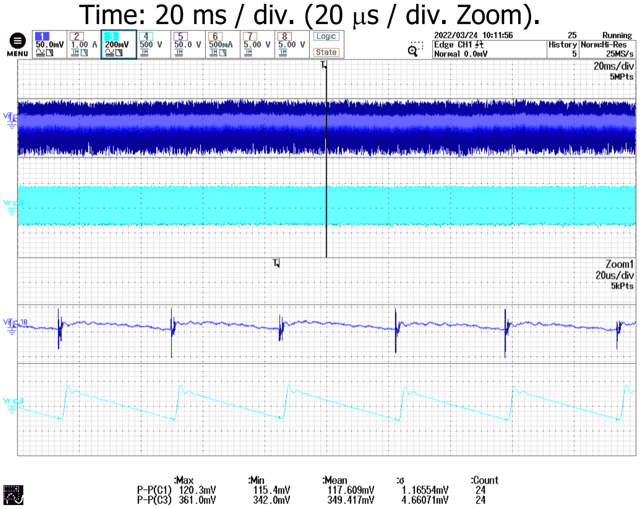
11.4.2.2 Output Voltage Ripple at 25 °C Ambient Temperature[41]



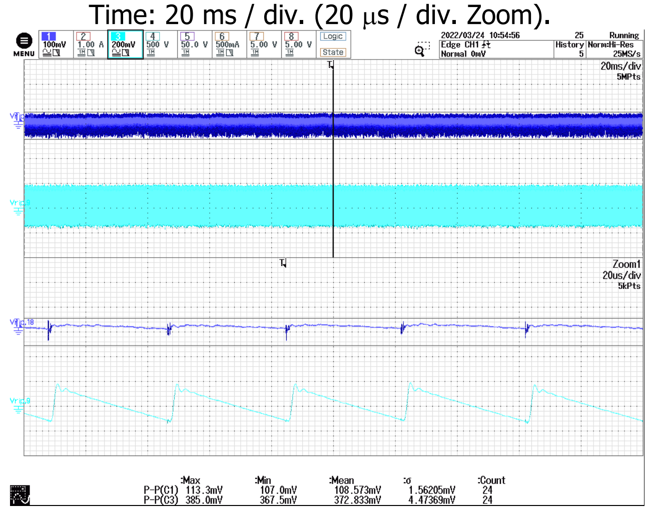
30 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



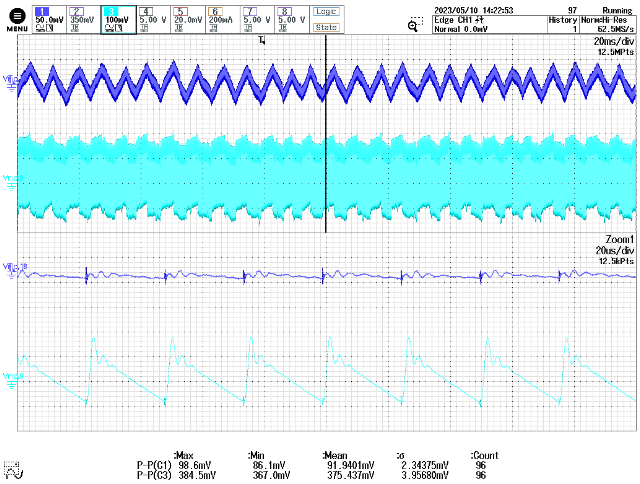
1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 100 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom)

Figure 76 – Output Voltage Ripple at 25 °C Ambient Temperature.

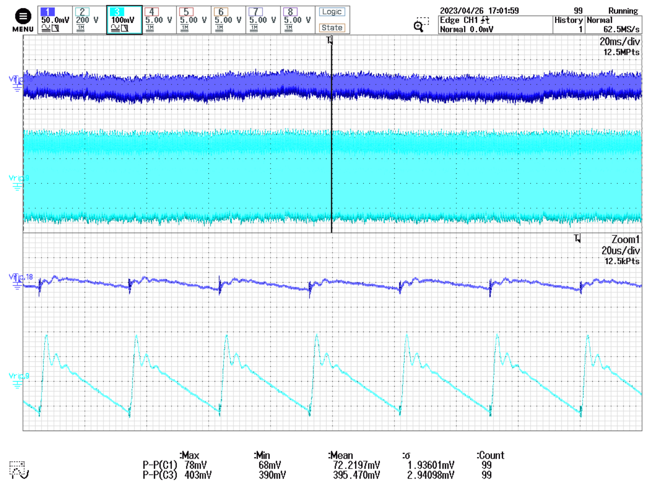
41 Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient Temperature[42]

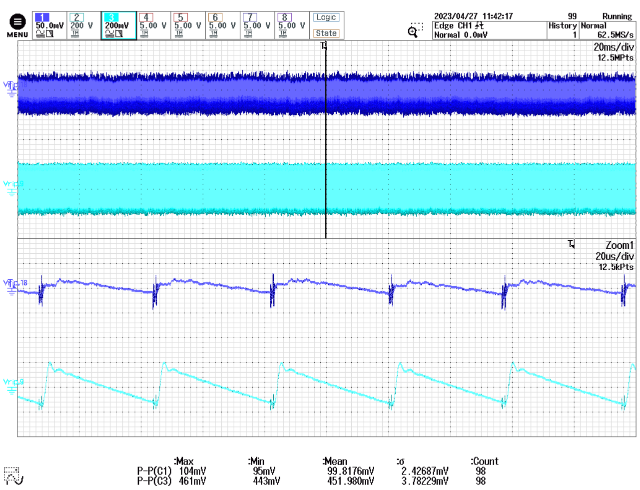
Probe extension using twisted pair wires was implemented for the test performed at -40 °C ambient temperature due to the inaccessibility of the probing point once placed inside the thermal chamber. To compensate for the effects of the probe extension, values shown on the figures below must be increased by 14.17 mV_{PP} for the 18 V output and must be decreased by 57.14 mV_{PP} for the 9V output.[43]



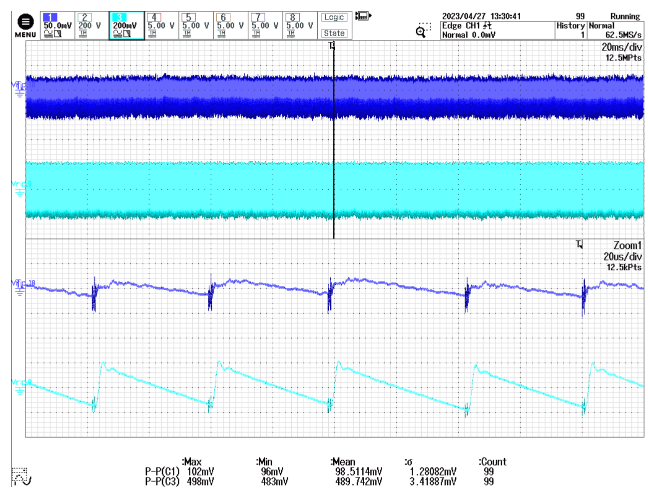
30 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



60 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 100 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



800 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 50 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom).



1000 V_{DC} Input, 18 V = Max. 9 V = Max. Output.
CH1: 18 V, 100 mV / div.
CH3: 9 V, 200 mV / div.
Time: 20 ms / div. (20 µs / div. Zoom)

Figure 77 – Output Voltage Ripple at -40 °C Ambient Temperature.

[42] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).
[43] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple measurements obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

11.4.3 Output Voltage Ripple vs. Load

Each line on the graphs represents the output voltage ripple vs. total output power of the unit under test when the 18V output load is maintained at a certain percentage while the 9 V output load is increased from its minimum to maximum loading condition.

11.4.3.1 30 V_{DC} Input

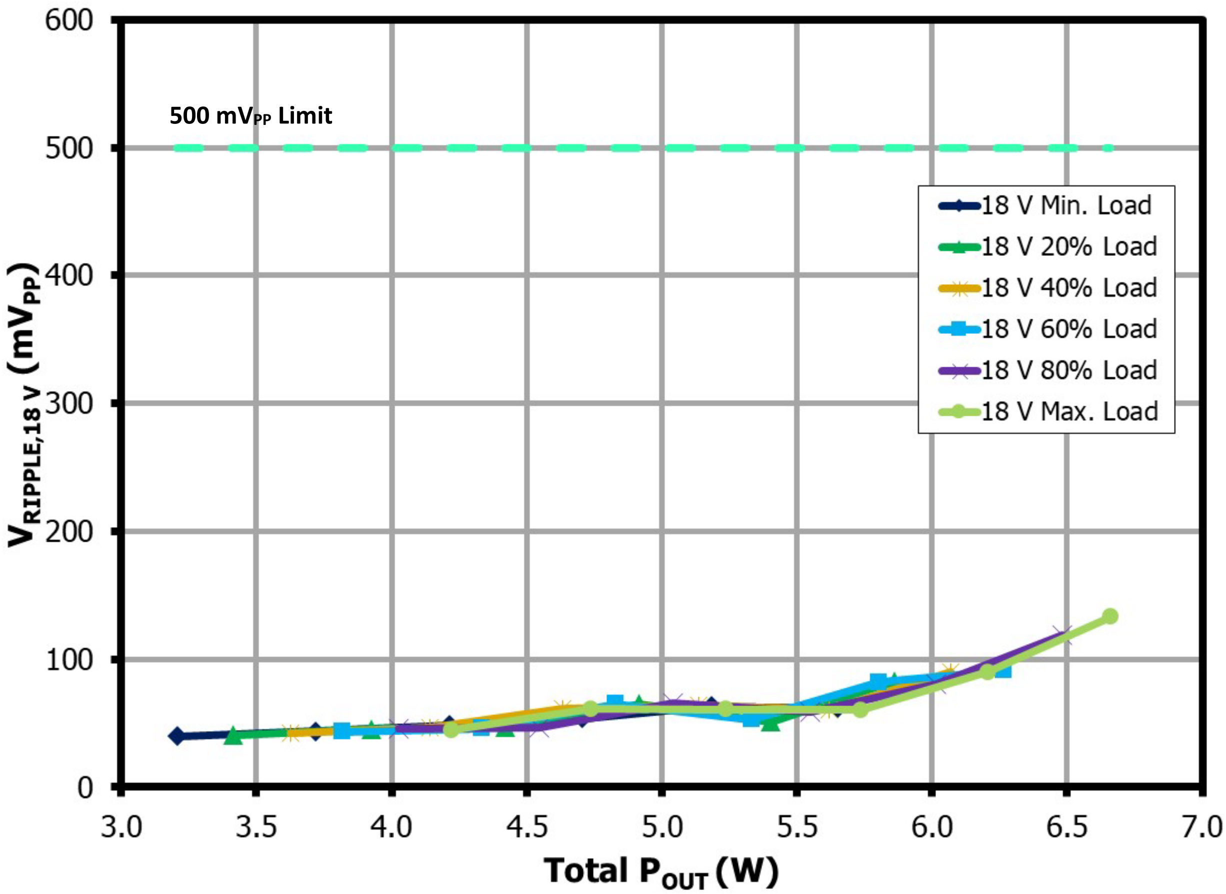


Figure 78 – 18 V Output Voltage Ripple vs. Total Output Power at 30 V_{DC} Input and 105 °C Ambient Temperature.

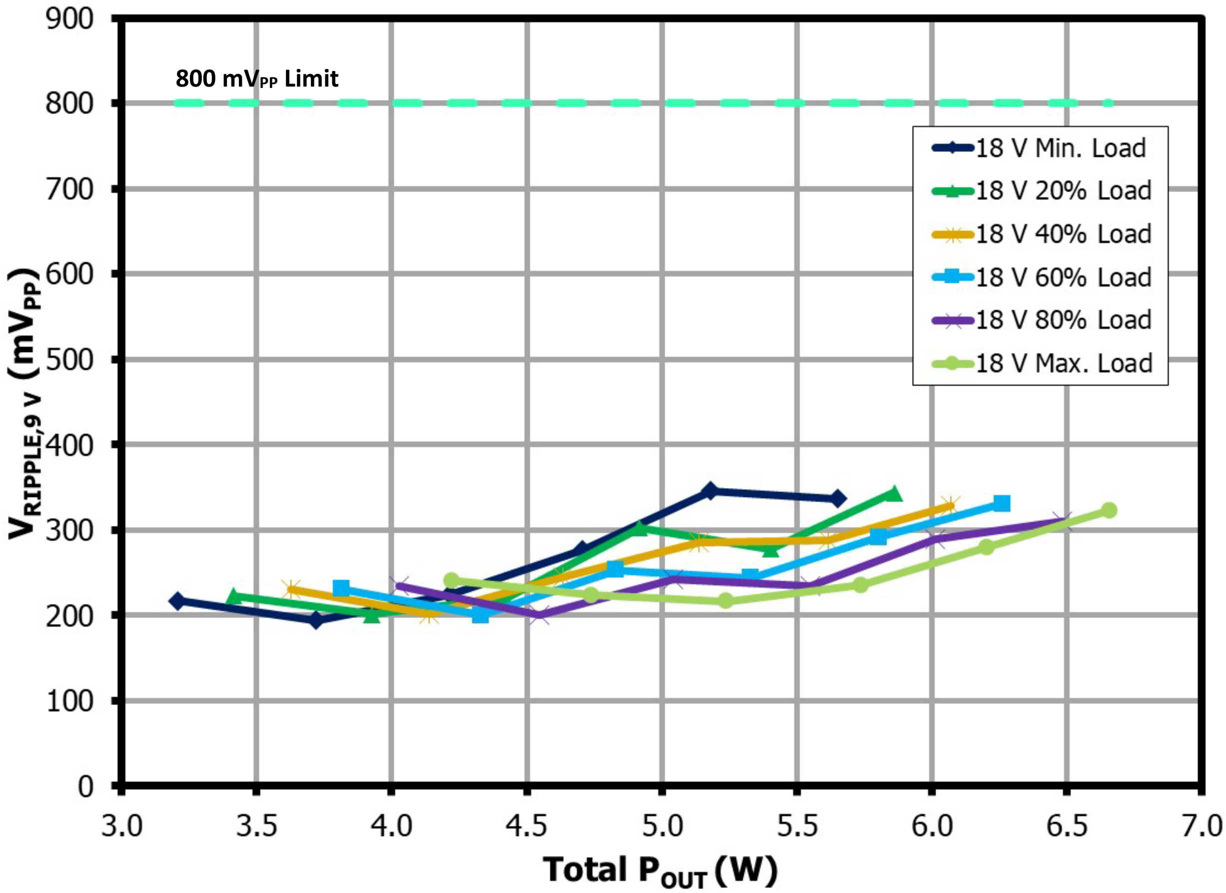


Figure 79 – 9 V Output Voltage Ripple vs. Total Output Power at 30 V_{DC} Input and 105 °C Ambient Temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 14.17 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[44]

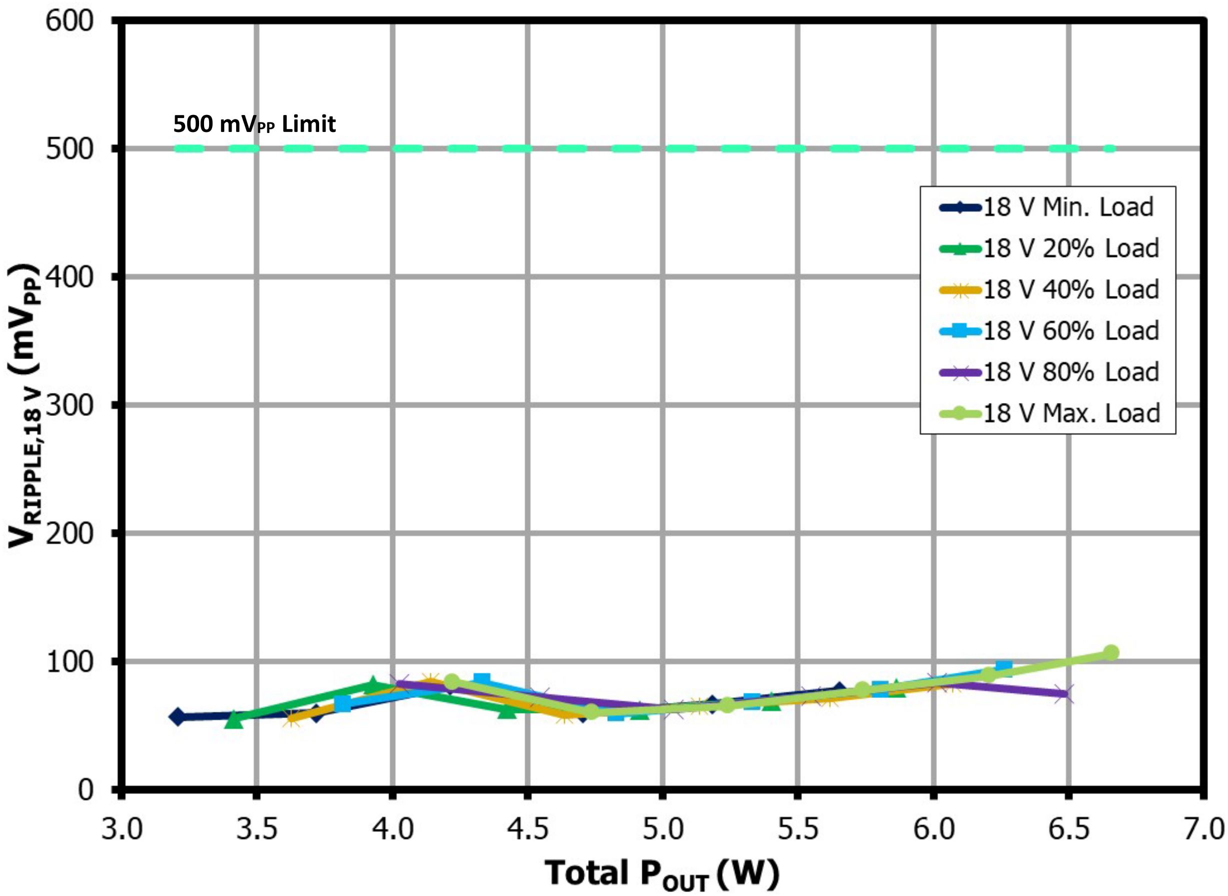


Figure 80 – 18 V Output Voltage Ripple vs. Total Output Power at 30 V_{DC} Input and -40 °C Ambient Temperature.

[44] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 57.14 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[45]

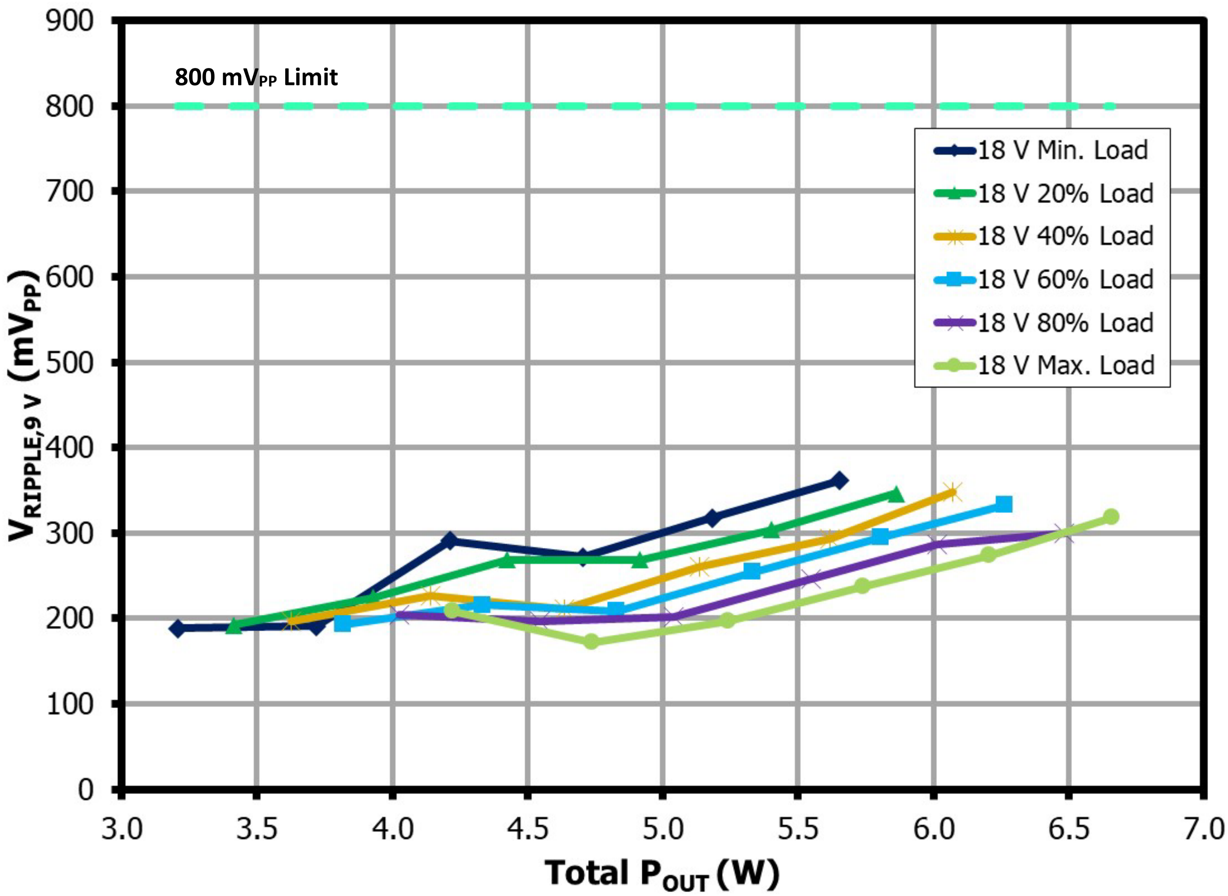


Figure 81 – 9 V Output Voltage Ripple vs. Total Output Power at 30 V_{DC} Input and -40 °C Ambient Temperature.

[45] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

11.4.3.2 60 V_{DC} Input

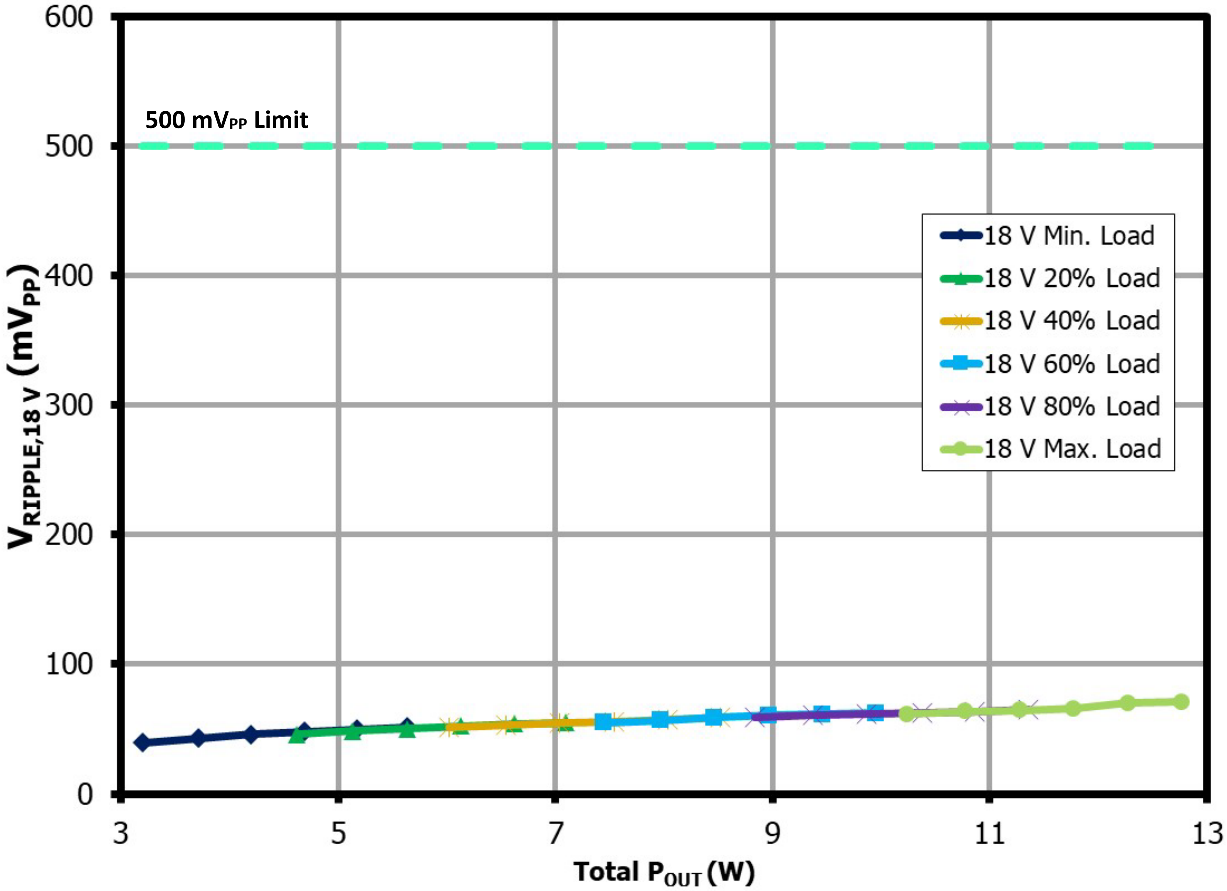


Figure 82 – 18 V Output Voltage Ripple vs. Total Output Power at 60 V_{DC} Input and 105 °C Ambient Temperature.

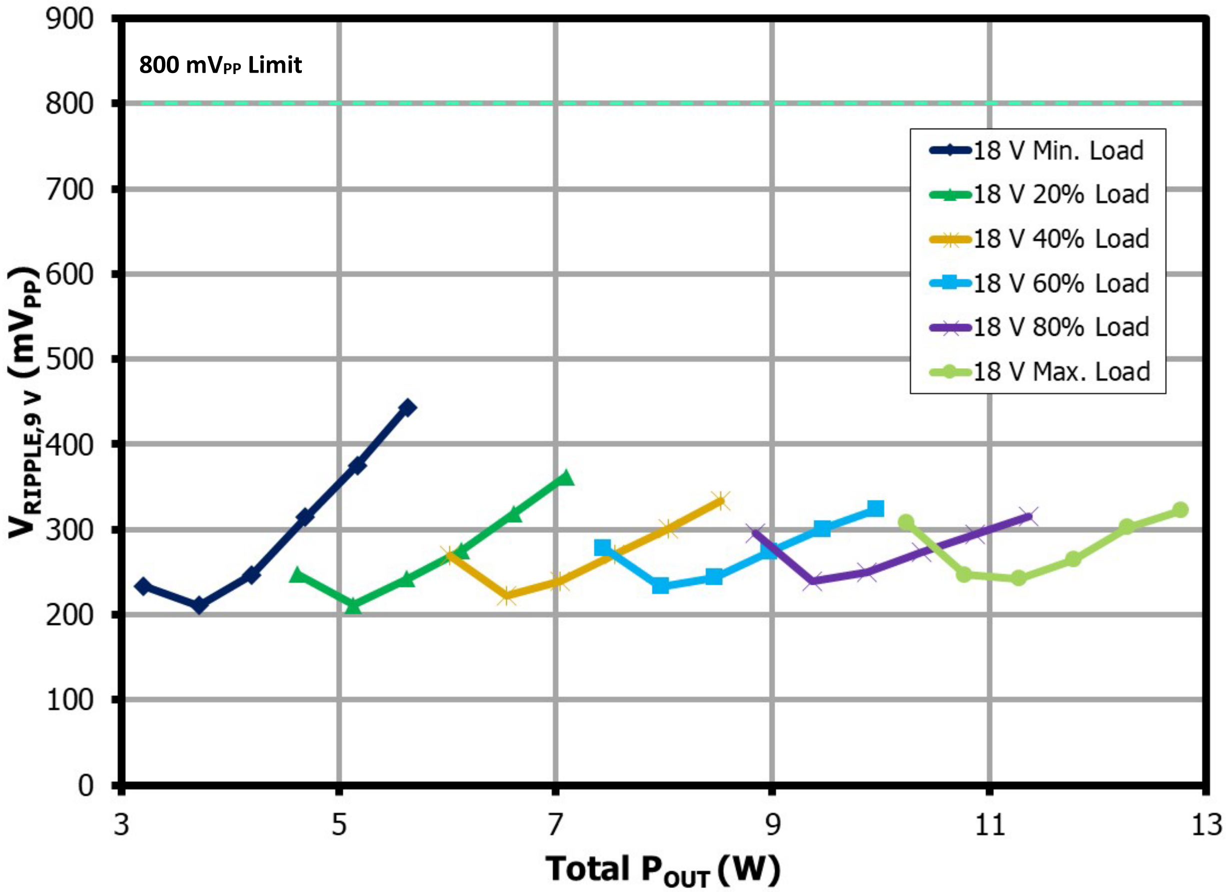


Figure 83 – 9 V Output Voltage Ripple vs. Total Output Power at 60 V_{DC} Input and 105 °C Ambient Temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 14.17 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[46]

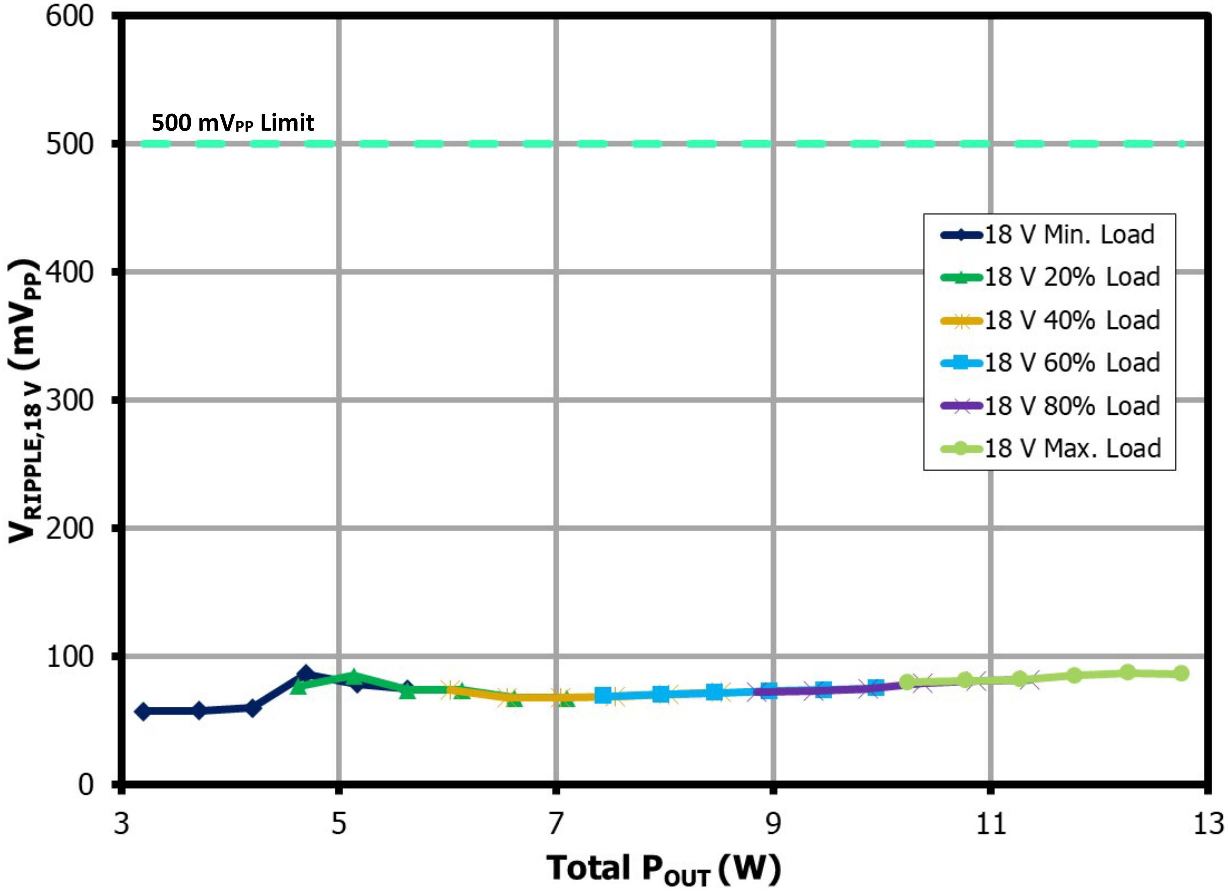


Figure 84 – 18 V Output Voltage Ripple vs. Total Output Power at 60 V_{DC} Input and -40 °C Ambient Temperature.

[46] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 57.14 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[47]

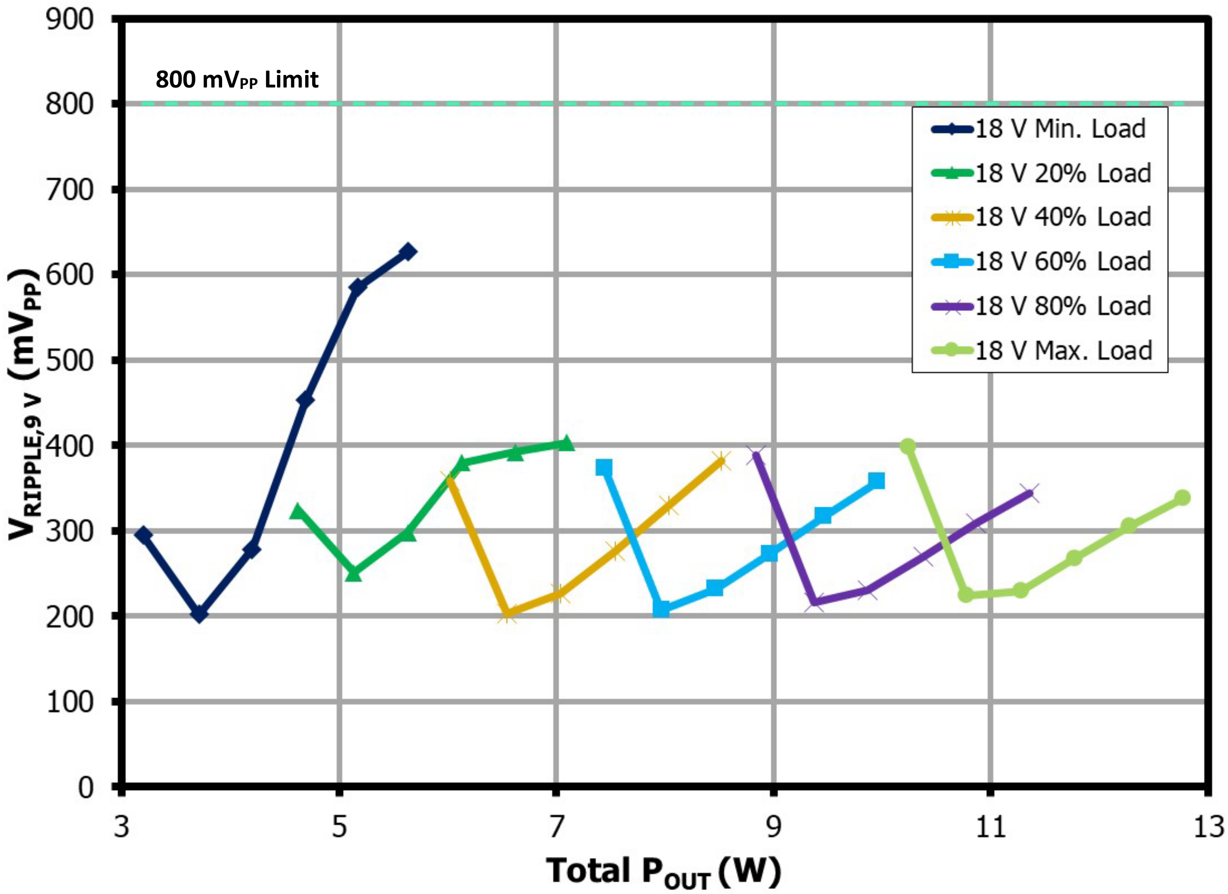


Figure 85 – 9 V Output Voltage Ripple vs. Total Output Power at 60 V_{DC} Input and -40 °C Ambient Temperature.

[47] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

11.4.3.3 800 V_{DC} Input

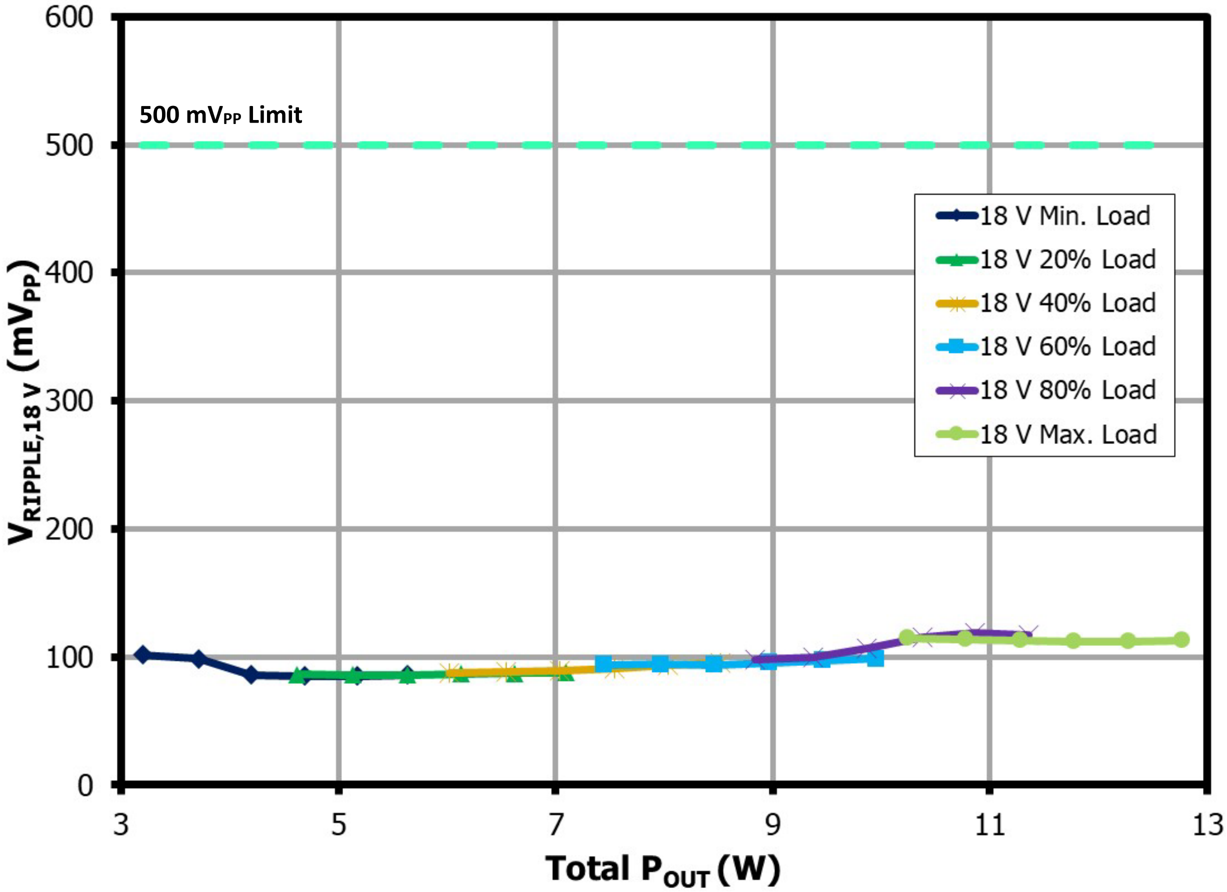


Figure 86 – 18 V Output Voltage Ripple vs. Total Output Power at 800 V_{DC} Input and 105 °C Ambient Temperature.

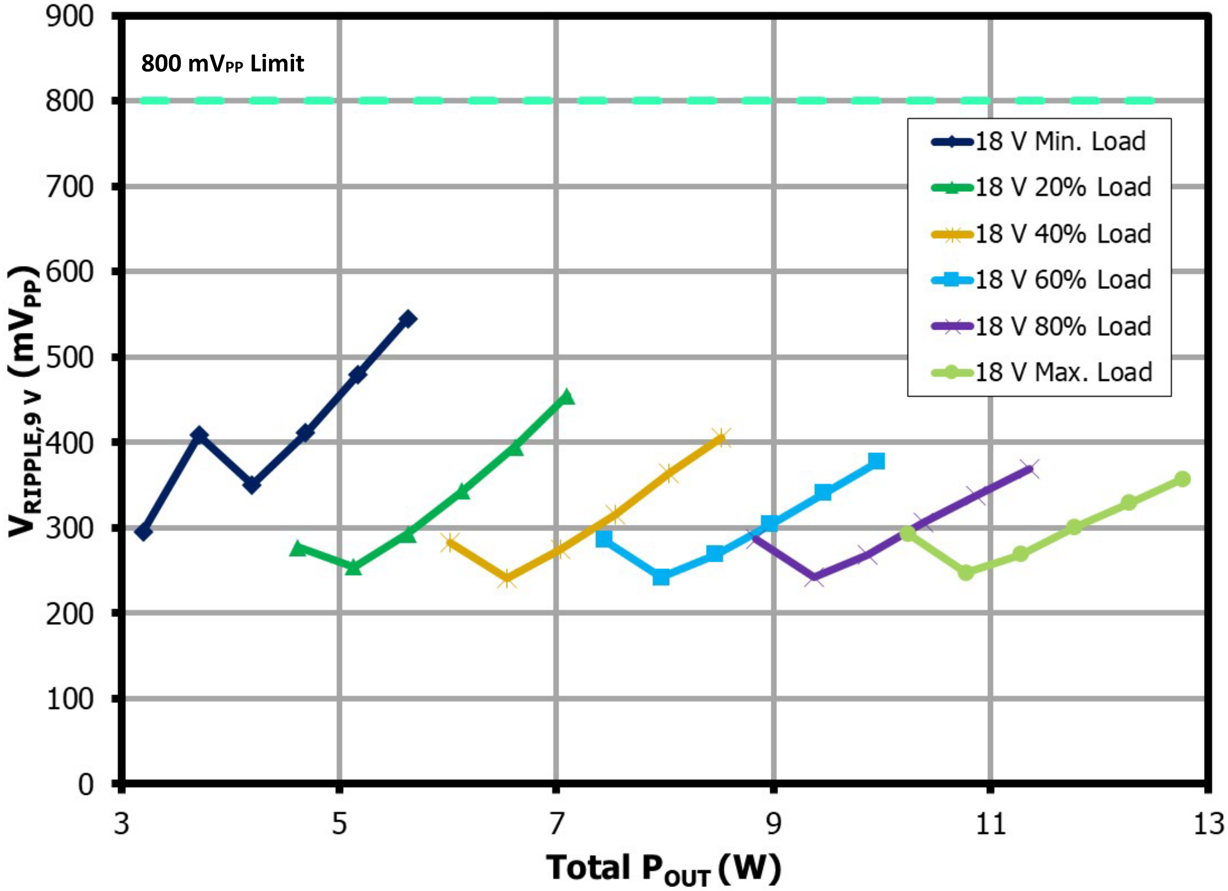


Figure 87 – 9 V Output Voltage Ripple vs. Total Output Power at 800 V_{DC} Input and 105 °C Ambient Temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 14.17 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[48]

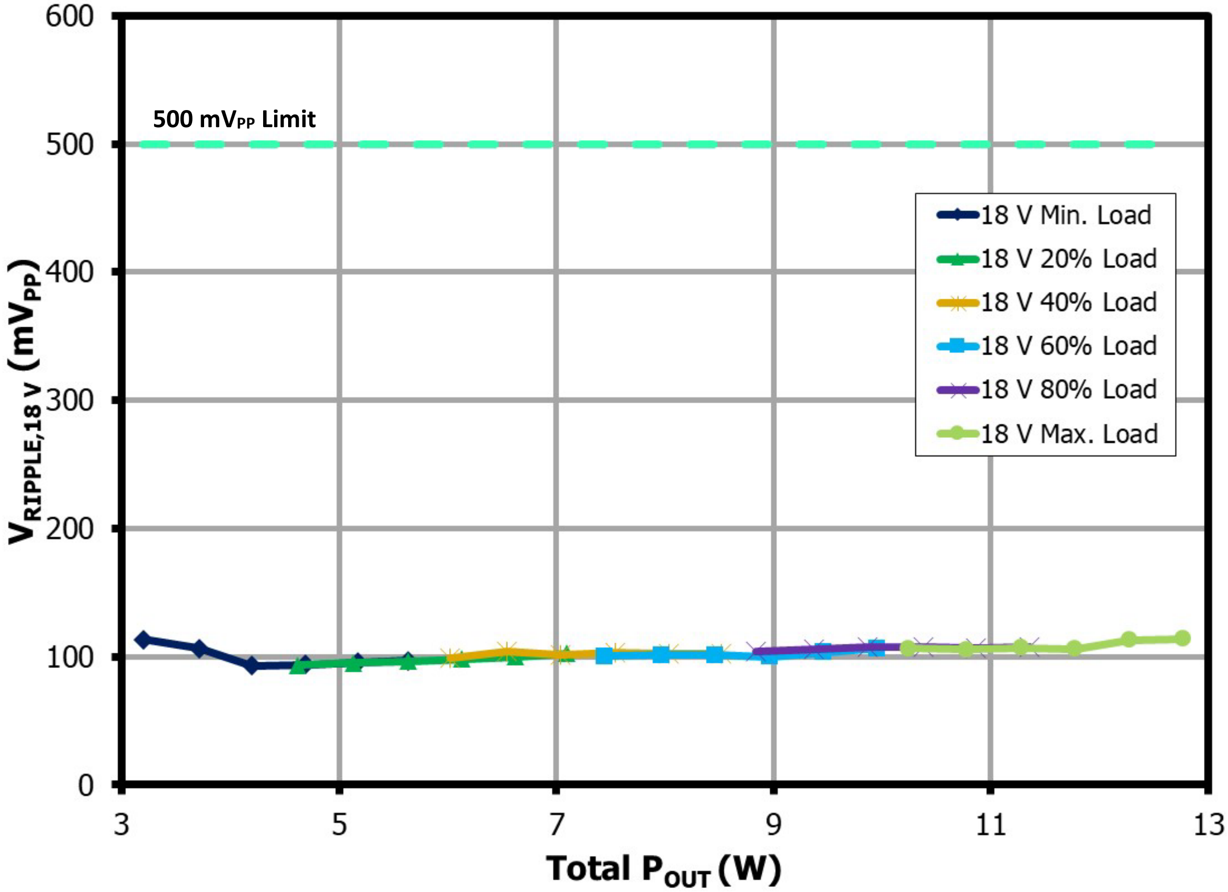


Figure 88 – 18 V Output Voltage Ripple vs. Total Output Power at 800 V_{DC} Input and -40 °C Ambient Temperature.

48 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 57.14 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[49]

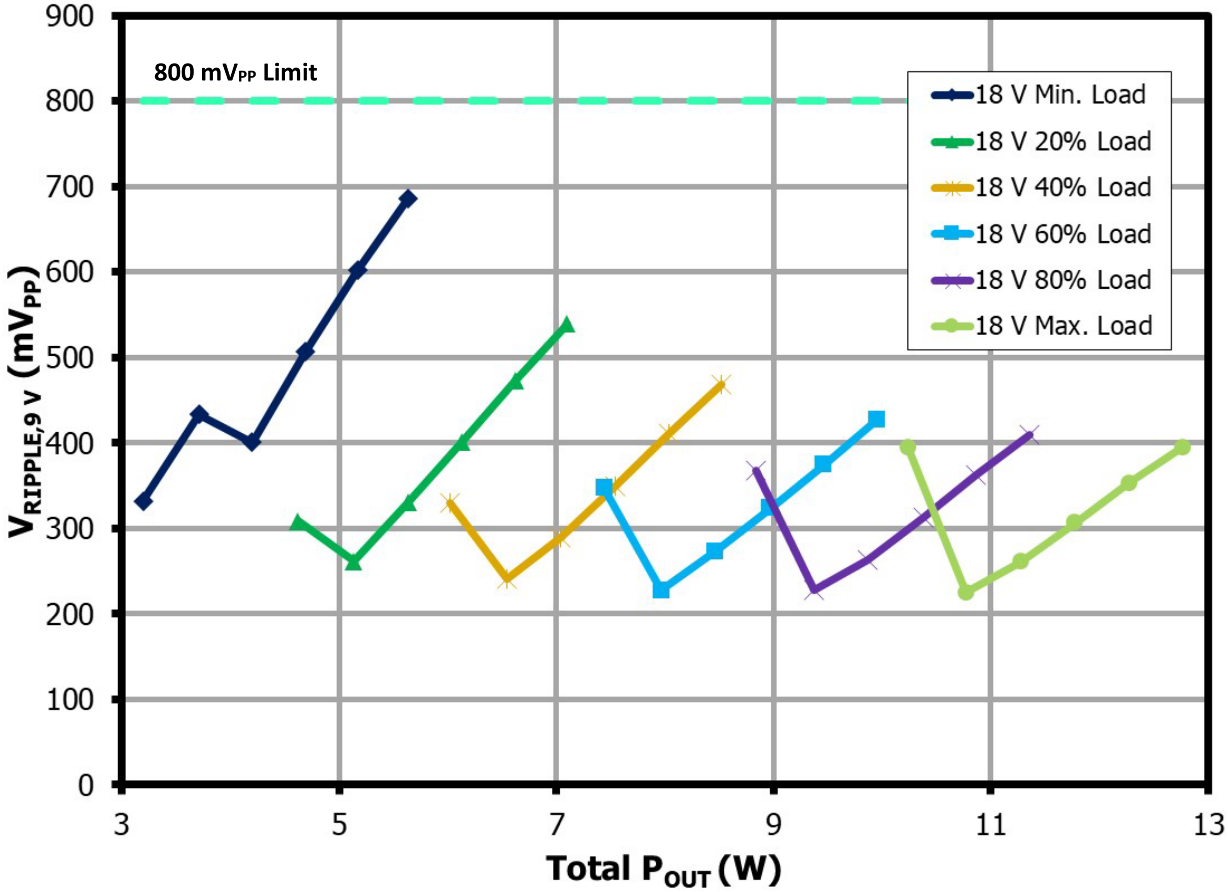


Figure 89 – 9 V Output Voltage Ripple vs. Total Output Power at 800 V_{DC} Input and -40 °C Ambient Temperature.

[49] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

11.4.3.4 1000 V_{DC} Input

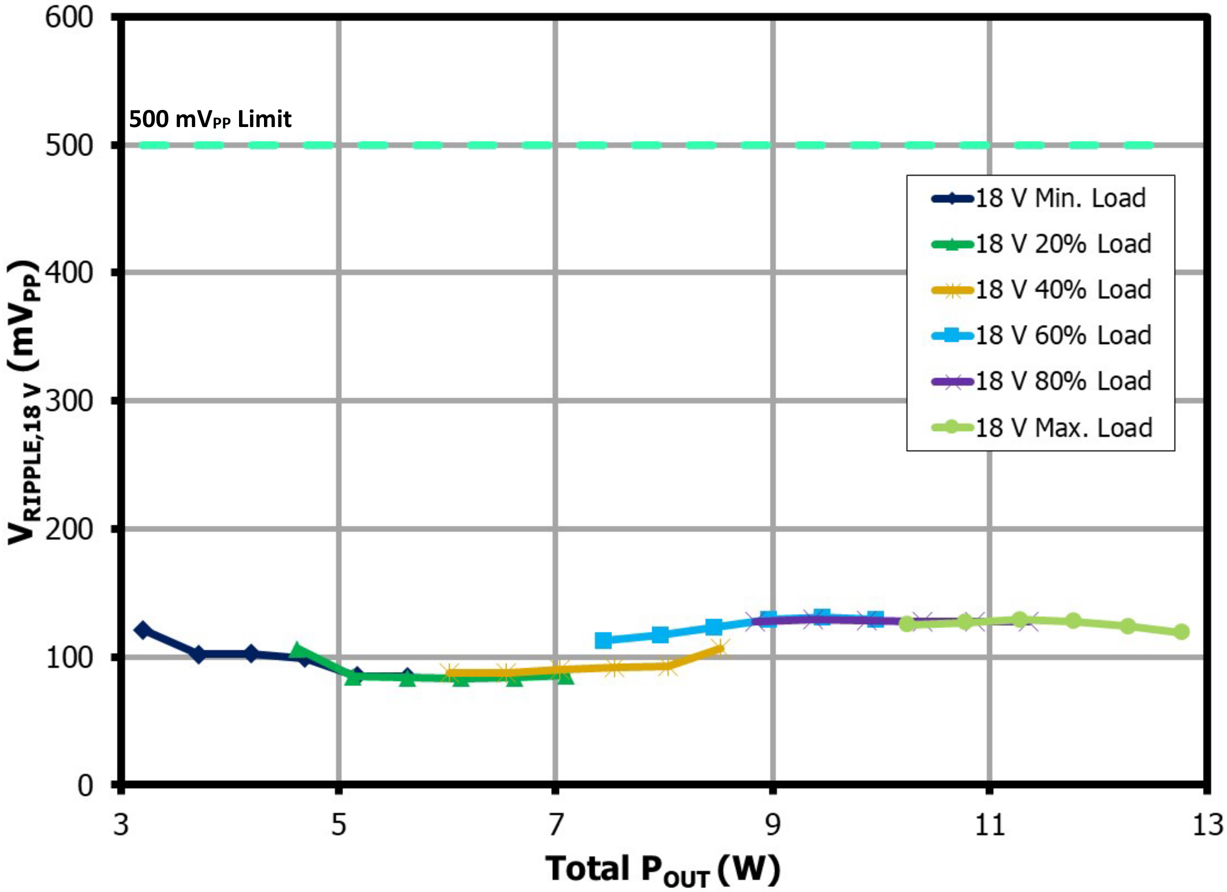


Figure 90 – 18 V Output Voltage Ripple vs. Total Output Power at 1000 V_{DC} Input and 105 °C Ambient Temperature.

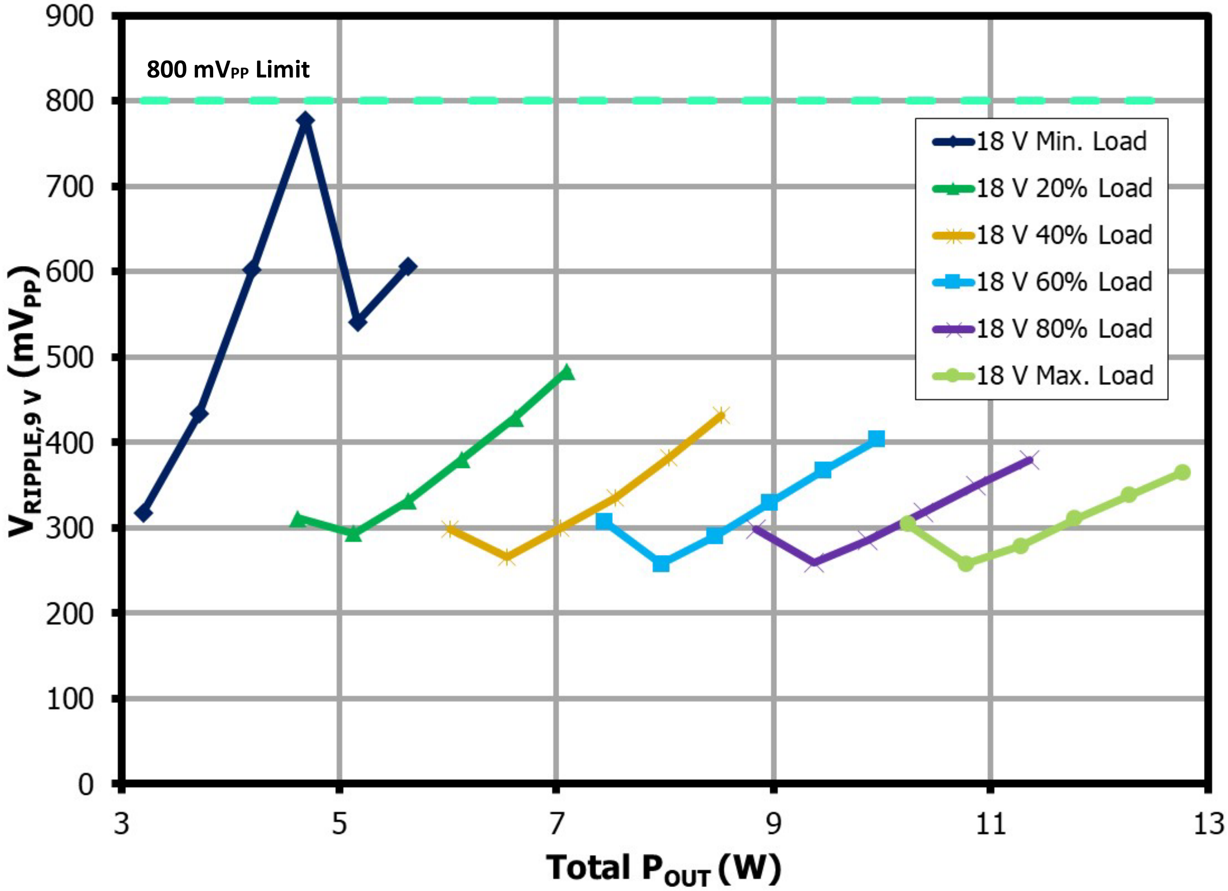


Figure 91 – 9 V Output Voltage Ripple vs. Total Output Power at 1000 V_{DC} Input and 105 °C Ambient Temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 14.17 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[50]

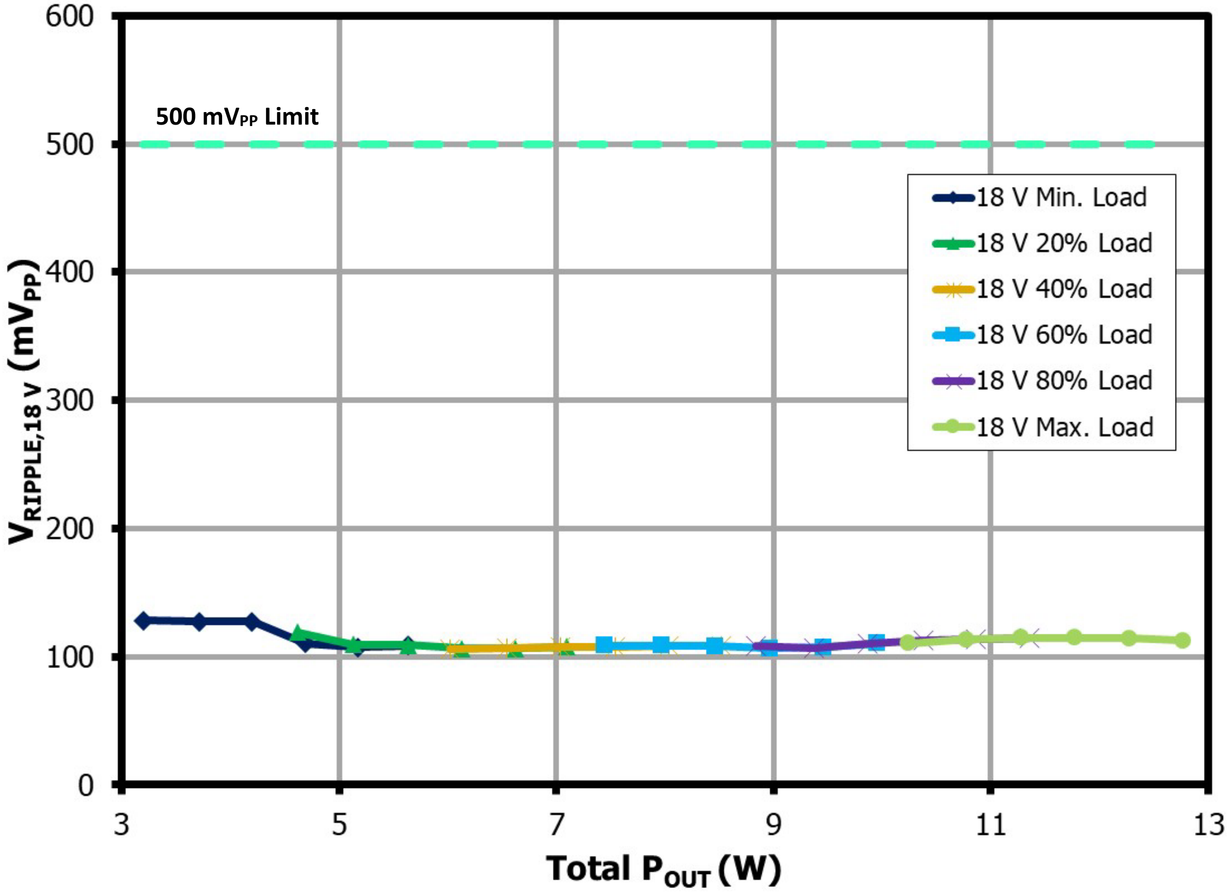


Figure 92 – 18 V Output Voltage Ripple vs. Total Output Power at 1000 V_{DC} Input and -40 °C Ambient Temperature.

[50] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

Output voltage ripple data at -40 °C ambient temperature shown below includes the 57.14 mV_{PP} offset to compensate for the effect the probe extensions had on the voltage ripple values.[51]

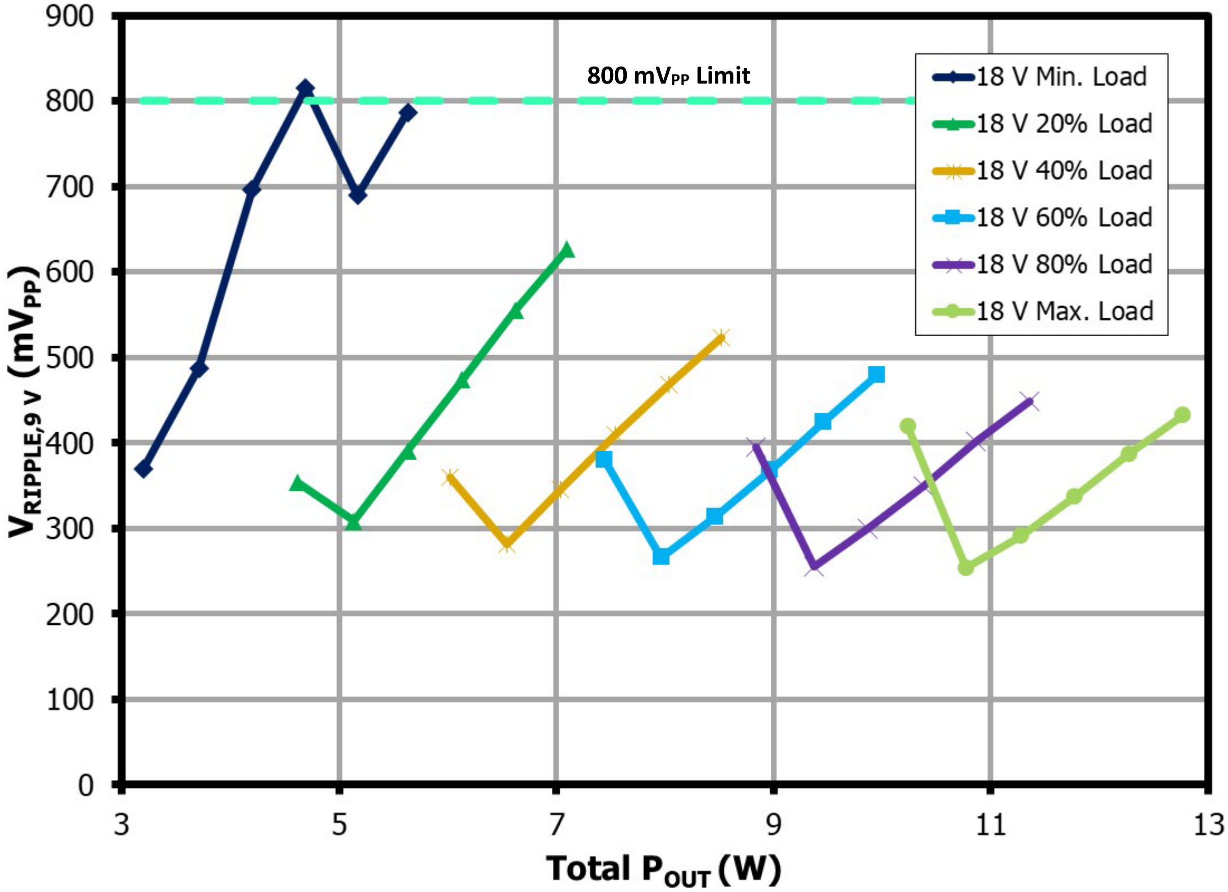


Figure 93 – 9 V Output Voltage Ripple vs. Total Output Power at 1000 V_{DC} Input and -40 °C Ambient Temperature.

[51] 14.17 mV_{PP} and 57.14 mV_{PP} are the average values of the difference between the 18 V and 9 V output voltage ripple values obtained, respectively, while using a short and extended probe at 25 °C ambient temperature.

12 Output Overload

12.1 *18 V Output Overload Capability*

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to desired ambient temperature for at least 30 minutes before turning on the unit under test. The unit was soaked for at least 20 minutes for every change in the input voltage during the start of each test sequence. Also, for every loading condition, unit under test was soaked for at least 60 seconds before the voltage and current measurements on the 18 V output were taken.

12.1.1 30 V_{DC} Input

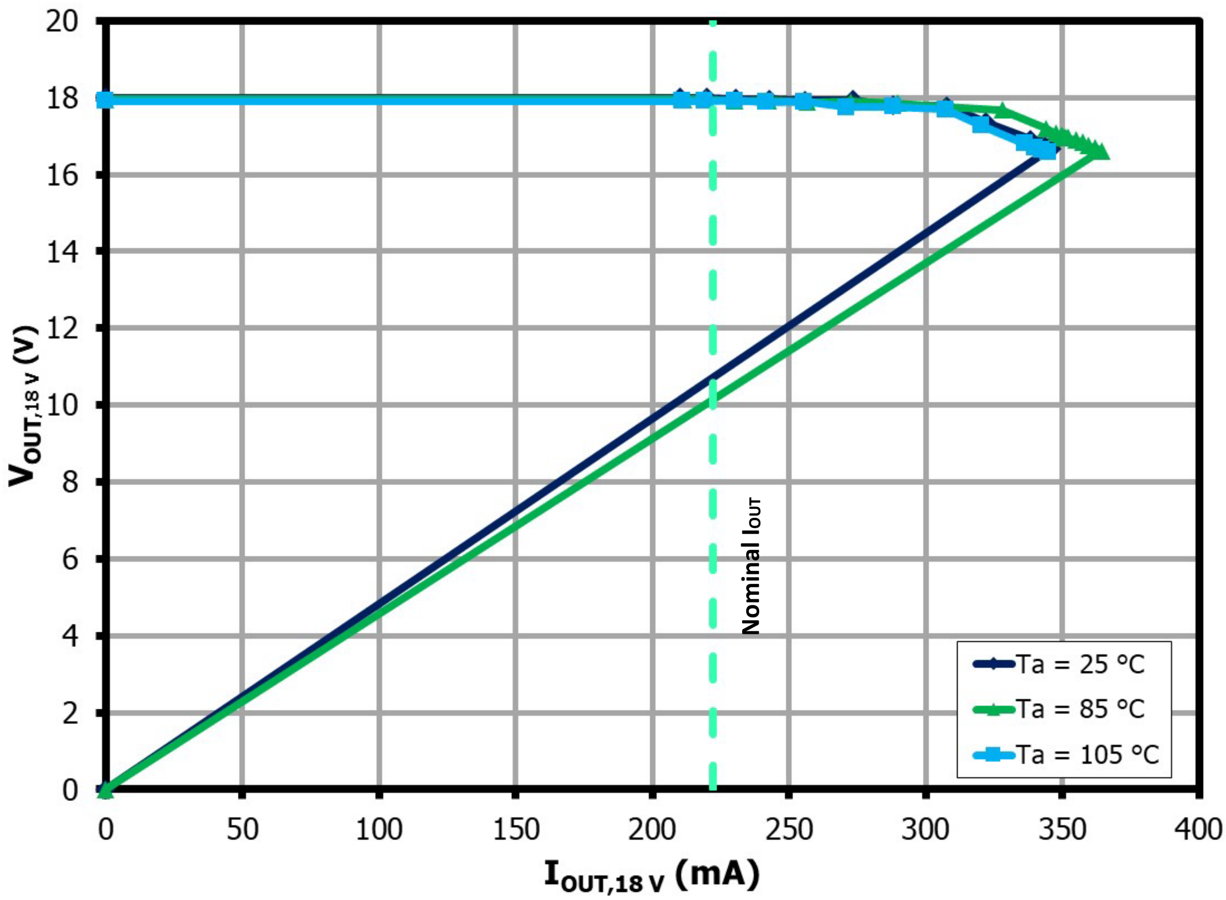


Figure 94 – 18 V Output Overload Curve at 30 V_{DC} Input.

12.1.2 60 V_{DC} Input

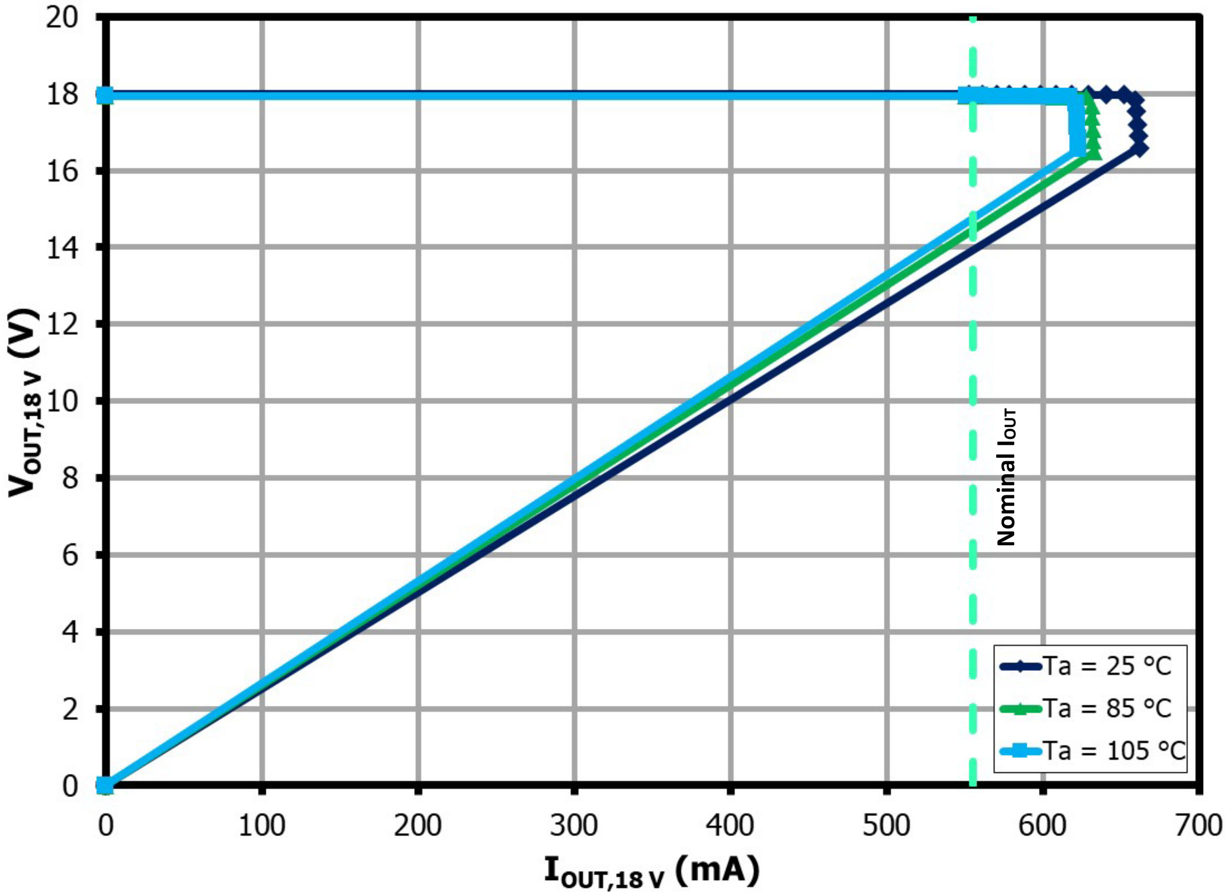


Figure 95 – 18 V Output Overload Curve at 60 V_{DC} Input.

12.1.3 800 V_{DC} Input

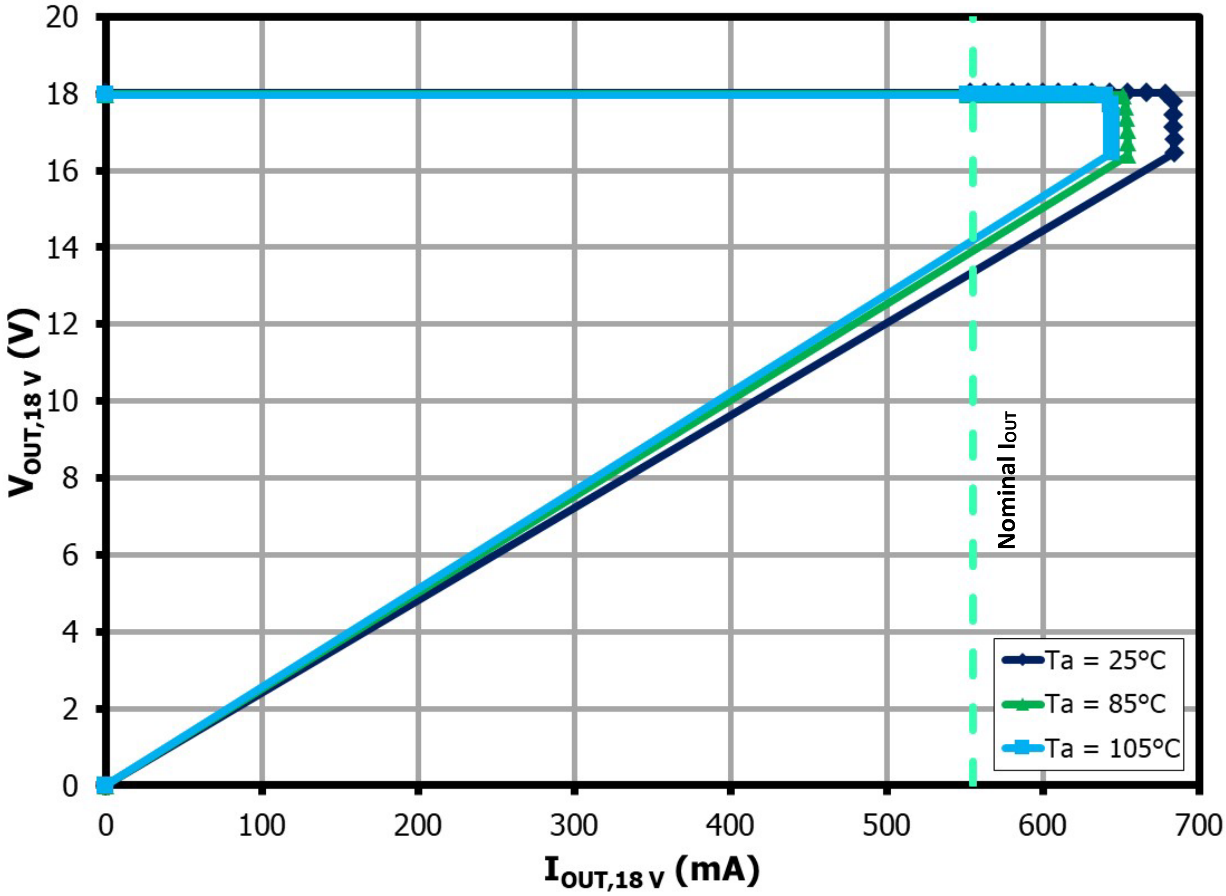


Figure 96 – 18 V Output Overload Curve at 800 V_{DC} Input.

12.1.4 1000 V_{DC} Input

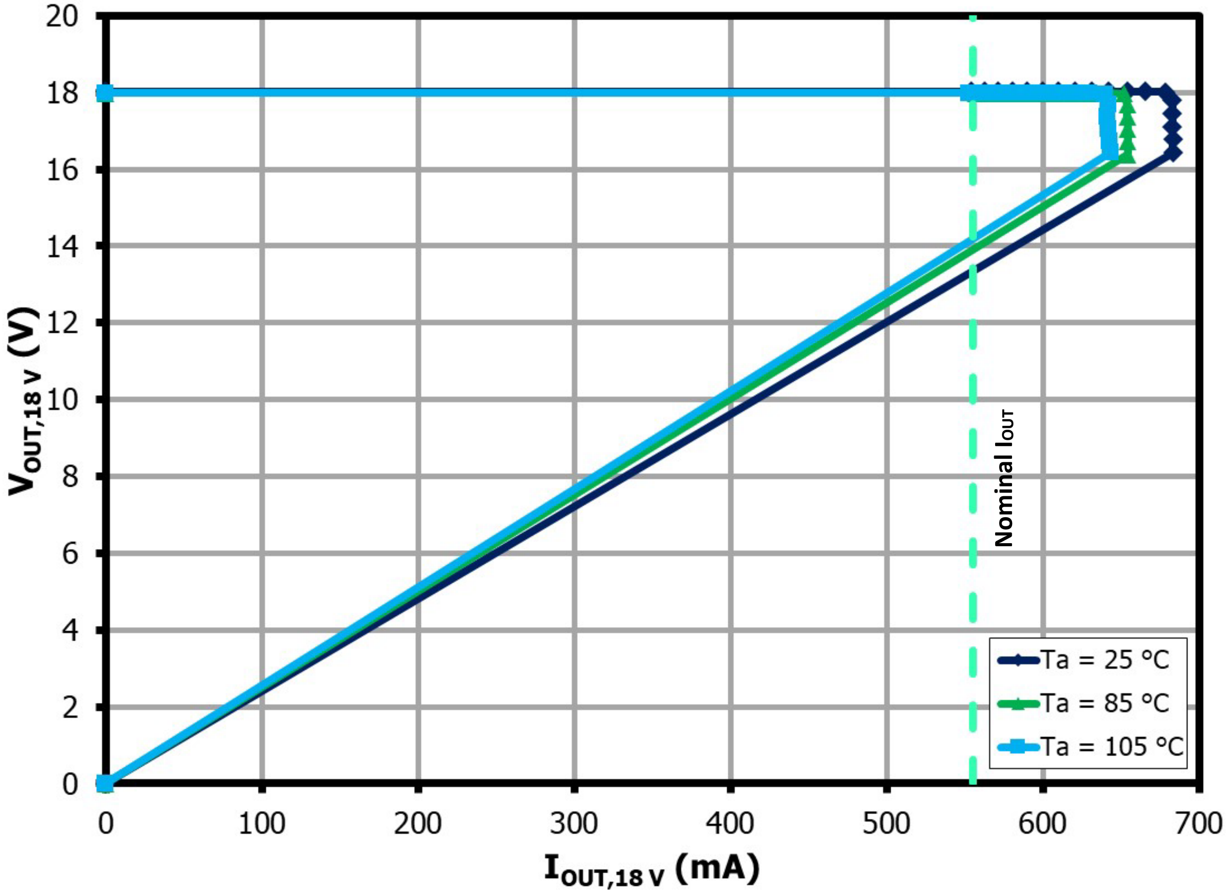


Figure 97 – 18 V Output Overload Curve at 1000 V_{DC} Input.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
09-May-22	JRL	1.0	Initial Release.	Apps & Mktg
20-Jul-22	JRL	1.1	Updated Figure 4 and 5. Updated Sections 2.2., 7.5 and 9.1.	Apps & Mktg
31-Jul-23	JS	2.0	Updated and added sections and figures for the data at -40 °C ambient temperature test condition.	Apps & Mktg

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